COMPAQ DESKPRO 386™
PERSONAL COMPUTER

TECHNICAL REFERENCE GUIDE, VOLUME II

COMPAQ

DESKPRO 386™

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Personal Computer
TECHNICAL REFERENCE GUIDE
Volume II

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COMPAQ Computer Corporation

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Chapter 5

KEYBOARDS

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Chapter 5
KEYBOARDS

5.1 INTRODUCTION

The keyboard is the primary means by which the user communicates with the system. Two keyboards are available with the COMPAQ DESKPRO 386: the COMPAQ 84-Key Keyboard and the COMPAQ Enhanced Keyboard. The 84-key keyboard offers full compatibility with similar keyboards used on 80286-based products. The enhanced keyboard is a 101-key keyboard (102-keys International) that offers additional features, such as a separate cursor control key cluster, additional function keys (F11 and F12), and enhanced programmability for make/break and repeating key functions.

Each of the keyboards offered with COMPAQ DESKPRO 386 contains a microprocessor that scans the keyboard for pressed keys. The microprocessor also monitors its communication line with the system. The communication line carries keyboard control commands from the system and keyboard scan and acknowledgment codes to the system. Keyboard scan codes are generated by the keyboard when a key is pressed or released. Typically, a Make code is generated when a key is pressed. A Break code is generated when the key is released.

Within this chapter, the term "system" refers to the keyboard controller (8042) on the system board.

Figure 5-1 is a functional block diagram of the keyboard, which is the same for both keyboards.

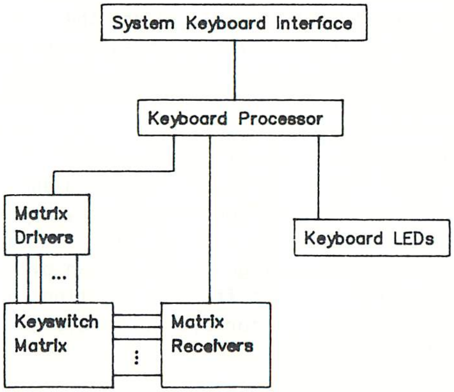


Figure 5-1. Keyboard Functional Block Diagram

5.2 KEYBOARD FEATURES

Both the 84-key and enhanced keyboards contain a first-in, first-out (FIFO) buffer and a repeating key function. The 84-key keyboard can store as many as 16 keycodes in its FIFO buffer. The enhanced keyboard is capable of storing 20 scan codes in its FIFO buffer. Keycodes are placed in the FIFO buffer when keys are pressed or released, if the keyboard is not able to immediately send the keycode to the system. When the keyboard is able to get the system's attention, it sends the keycodes stored in the FIFO buffer to the system in the order in which the keys were pressed.

When two keys are pressed simultaneously, the keyboard processes the first keycode detected and stores the second in the FIFO buffer. If any key is pressed while the FIFO buffer is full, the corresponding keycode is not generated and an overrun code (00h) is stored in the buffer. A location in the FIFO buffer is reserved for overrun conditions.

Another important feature of the keyboards is the repeating key function. This feature allows the keyboards to repeatedly generate and send the Make code to the system as long as the key is held down. The rate at which Make codes are generated can be programmed on both keyboards. The 84-key keyboard has a fixed set of keys (most keys except for a few special function keys) that are capable of the repeat operation. The enhanced keyboard allows the user to designate a particular set of keys to perform the repeat operations. The set of keys that can perform the repeat operation is programmable by the system via commands.

Figure 5-2 shows the 84-key keyboard. Figure 5-3 shows the enhanced keyboard.

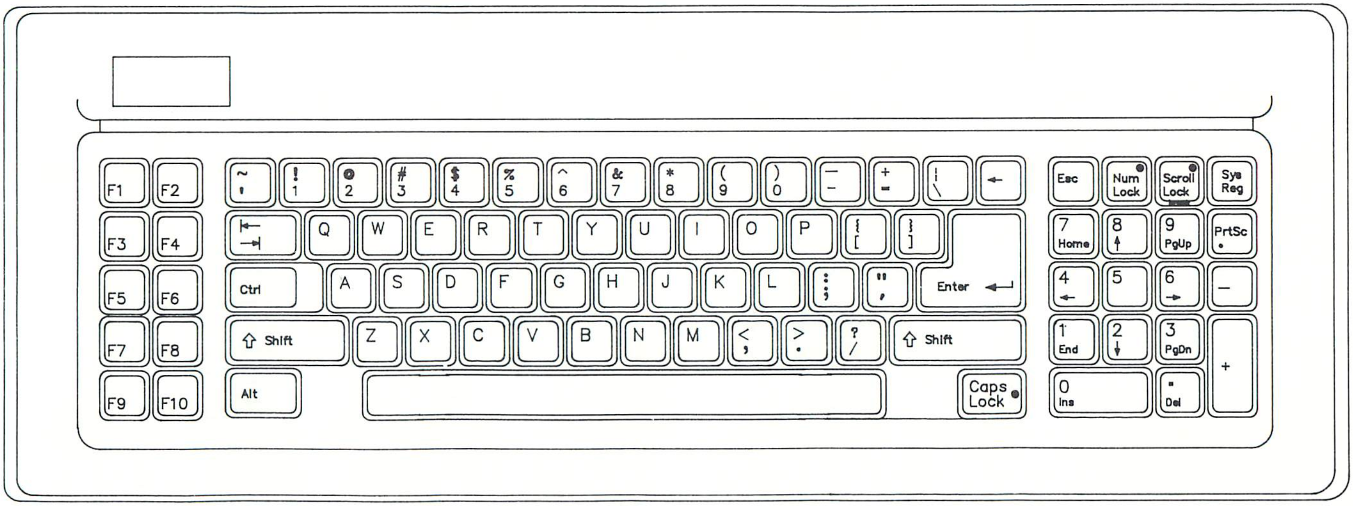


Figure 5-2. 84-Key Keyboard

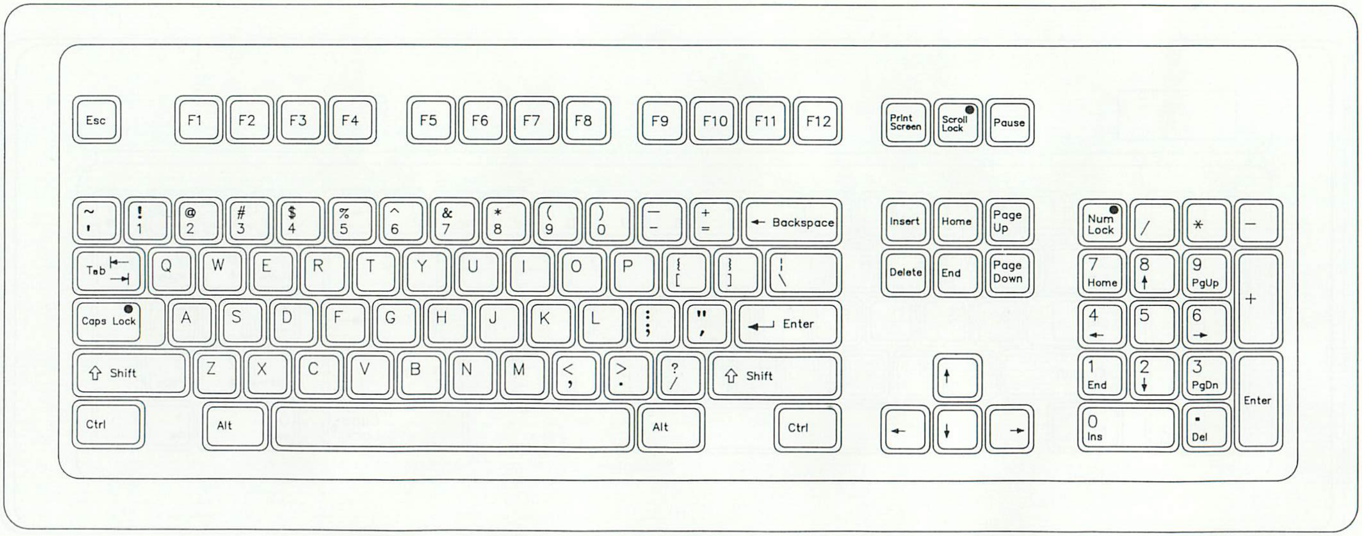


Figure 5-3. Enhanced Keyboard

5.3 KEYBOARD COMMUNICATIONS INTERFACE

Both keyboards use a bidirectional, synchronous serial interface for communications with the system. The keyboard cable is a 4-conductor, shielded cable.

The keyboard data (KBDDATA) and keyboard clock (KBDCLK) signals use TTL-compatible voltage levels, with open-collector drivers.

Communication between the system and the keyboards is implemented with a protocol method, shown in Figure 5-4.

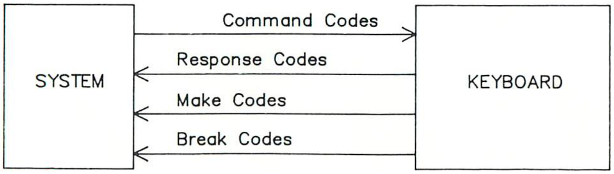


Figure 5-4. Keyboard Communication Protocol

Table 5-1. Keyboard Specifications for Both Keyboards

Voltage	+ 5 VDC
Tolerance	± 10%
Current	250 mA (maximum)
Cable Length:	
Coiled	38 in. (97 cm)
Extended	75 in. (190 cm)

Communication Protocol

The communications link between the system and keyboard is bidirectional. For status information, the system controls the communications link. For data communication, either the system or the keyboard may control the data line, but not at the same time. The clock line is always controlled by the keyboard.

Commands from the System

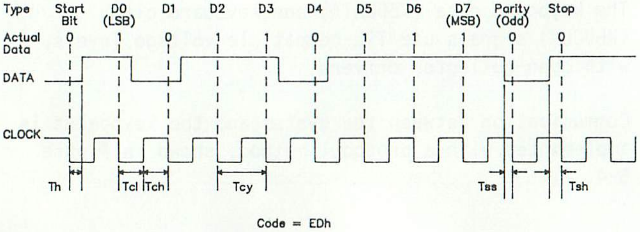
The system can send, at any time, various commands to the keyboard. When the keyboard is transmitting to the system, the system first clamps the clock signal line to request a keyboard transmission halt. To ensure that the keyboard recognizes the system's request, the clock line must remain low (0) for at least 60 ms. When the keyboard's transmission is past the rising edge of the parity bit's clock pulse, the keyboard will complete its transmission before loading the system command.

When the system is ready to transmit a command to the keyboard, it sets the data line low (0). This action serves as both a Request-to-Send and a Start bit. Upon detecting the data line low, the system sets the clock line low, causing the Start bit to be clocked out of the system. The system then places the least-significant bit (LSB, data bit 0) on the data line. This action causes the keyboard to raise and lower the clock line. This process continues until all 8 data bits are clocked out of the system.

After all data bits are clocked out of the system, the system places an Odd Parity bit on the data line. The keyboard repeats its clocking of the parity bit as before. The keyboard then sets the data line low and clocks this line to the system for a Stop bit. When the keyboard receives the Stop bit, the system sets the clock line low to inhibit the keyboard while it is processing the received data.

After the keyboard receives a system command, the keyboard returns an ACK code to the system. For more information on the ACK code, see "84-Key Keyboard Responses to the System" in this chapter. If a parity error or timeout occurs, a Resend command is sent to the system.

Figure 5-5 shows the timing of system-to-keyboard transmissions.



Symbol	Parameter	Minimum	Maximum
Tcy	Cycle Time	60 us	80 us
Tcl	Clock Low	25 us	35 us
Tch	Clock High	25 us	45 us
Th	Data Hold	0 us	25 us
Tss	Stop Bit Setup	8 us	20 us
Tsh	Stop Bit Hold	15 us	25 us

Notes:
1. DATA signal clamped low by system, used as RTC signal.
2. DATA signal clamped low by keyboard as Stop Bit.
3. CLOCK signal clamped low by system to inhibit keyboard.

Figure 5-5. System-to-Keyboard Timing Transmissions

5.4 KEYBOARD FUNCTIONS

This section describes the unique function of each keyboard. These descriptions refer to the domestic keyboards only because key numbers differ for the various international keyboards. The layouts of the international keyboards are shown in Appendix B.

84-Key Keyboard

The keyboard controller generates a fixed set of Make and Break keycodes for each of the keys on the 84-key keyboard. When a key is pressed, the keyboard controller sends that key's Make keycode to the system.

When a key is released, the keyboard controller sends two keycodes: F0h, followed by that key's make keycode to the system.

For a layout of the 84-key keyboard and the position number assigned to each key, see Figure 5-6. Table 5-2 lists the Make codes for each key on the 84-key keyboard.

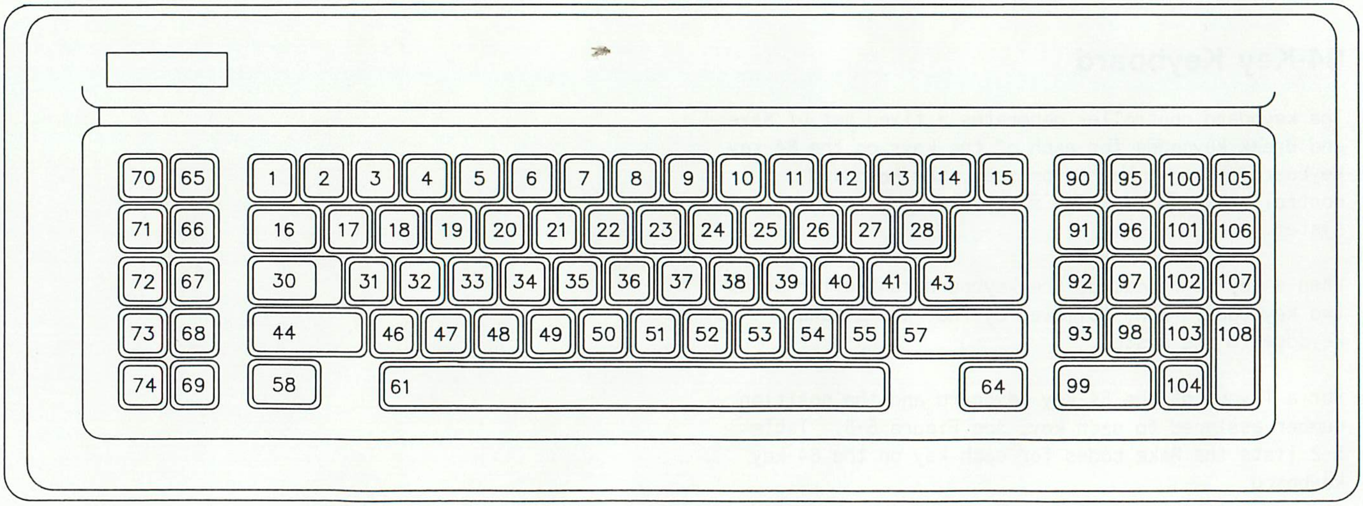


Figure 5-6. Assigned Position Number for Each Key on the 84-Key Keyboard

Table 5-2. Keycap Data for the 84-Key Keyboard

Location	Legend (Top of Cap)		Make Code
1	~	`	0E
2	!	1	16
3	@	2	1E
4	#	3	26
5	$	4	25
6	%	5	2E
7	^	6	36
8	&	7	3D
9	*	8	3E
10	(	9	46
11	)	0	45
12	_	-	4E
13	+	=	55
14	|	\	5D
15	(Backspace)		66
16	(Back Tab)	(Tab)	0D
17	Q		15
18	W		1D
19	E		24
20	R		2D
21	T		2C
22	Y		35
23	U		3C
24	I		43
25	O		44

(Continued)

Table 5-2. Keycap Data for 84-Key Keyboard

Location	Legend (Top of Cap)		Make Code
26	P		4D
27	{	[	54
28	}	]	5B
30	Ctrl		14
31	A		1C
32	S		1B
33	D		23
34	F		2B
35	G		34
36	H		33
37	J		3B
38	K		42
39	L		4B
40	:	;	4C
41	"	'	52
43	Enter		5A
44	Left Shift		12
46	Z		1A
47	X		22
48	C		21
49	V		2A
50	B		32
51	N		31
52	M		3A
53	<	,	41

(Continued)

Table 5-2. Keycap Data for 84-Key Keyboard

Location	Legend (Top of Cap)	Make Code
54	> .	49
55	? /	4A
57	(Right) Shift	59
58	Alt	11
61	(Space Bar)	29
64	Caps Lock	58
65	F2	06
66	F4	0C
67	F6	0B
68	F8	0A
69	F10	09
70	F1	05
71	F3	04
72	F5	03
73	F7	83
74	F9	01
90	Esc	76
91	7 Home	6C
92	4 (Left Arrow)	6B
93	1 End	69
95	Num Lock	77
96	8 (Up Arrow)	75
97	5	73
98	2 (Down Arrow)	72
99	0 Ins	70

(Continued)

Table 5-2. Keycap Data for 84-Key Keyboard (Concluded)

Location	Legend (Top of Cap)	Make Code
100	Scroll Lock	7E
101	9 PgUp	7D
102	6 (Right Arrow)	74
103	3 PgDn	7A
104	. Del	71
105	Sys Req	84
106	Print Screen *	7C
107	-	7B
108	+	79

System/Keyboard Commands and Acknowledgments

Those commands sent by the system are listed in Table 5-3.

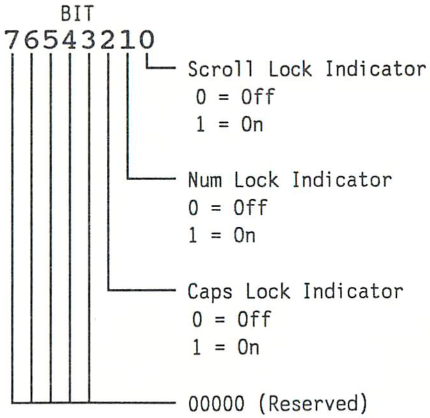
Table 5-3. System Commands to the Keyboard

Code	Function
EDh	Set Status Indicators
EEh	Echo Command (Diagnostic Aid)
EFh..F2h	Reserved--No operation
F3h	Set Key Repeat Rate
F4h	Enable the Keyboard
F5h	Disable Keyboard Scanning
F6h	Set Default Conditions
F7h..FDh	Reserved--No operation
FEh	Resend Command
FFh	Reset Command

SET STATUS INDICATORS (EDh)

The Set Status Indicators command (EDh) is a 2-byte command used to change the state of the keyboard's LED indicators. After receiving this command, the keyboard halts scanning, returns an ACK code to the system, and waits for the system to send the option byte. The option byte indicates which LED indicators are to be affected.

When the option byte is received, the keyboard sets the status indicator, returns an ACK code, and resumes scanning. If another command is received while the keyboard is waiting for the option byte, the Set Status Indicators command will be aborted and the new command will be executed. The status byte is formatted as follows:



ECHO (EEh)

The Echo command (EEh) is used for diagnostics. After receiving this command, the keyboard returns an Echo response (EEh).

NOP (EFh..F2h)

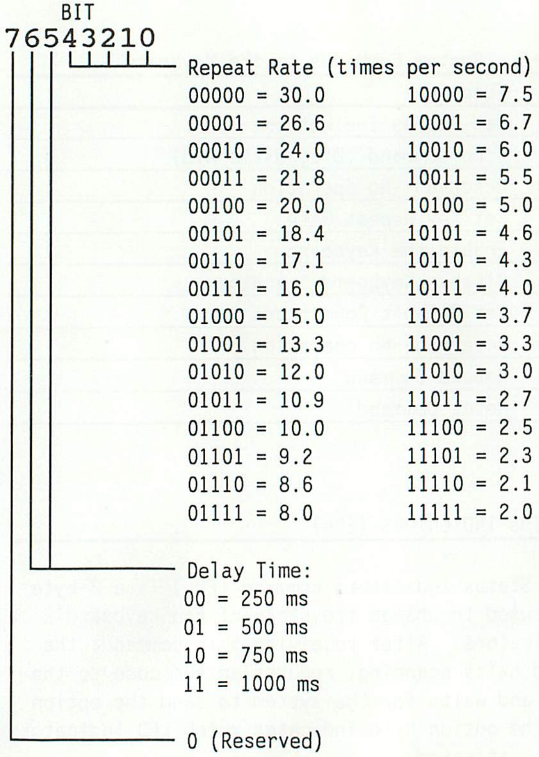
The keyboard responds to the NOP command with an ACK code. No other action is taken.

SET KEY REPEAT RATE (F3h)

The Set Key Repeat Rate command (F3h) is a 2-byte command that changes the key-repeat delay and rate values. This command functions similarly to the Set Status Indicator command (EDh).

Once the Set Key Repeat Rate command is received by the keyboard, the keyboard stops scanning and returns an ACK code. The system then sends a byte that contains the repeat rate and delay time values. The repeat rate is the number of times the key is repeated every second. The delay time is the length of time a key must be held down before the key repeat function begins. The keyboard then returns an ACK code and remains in the previous keyboard scan state, enabled or disabled.

The format for the Set Key Repeat Rate/Delay Time byte is as follows:



Repeat Rate (times per second)

00000 = 30.0	10000 = 7.5
00001 = 26.6	10001 = 6.7
00010 = 24.0	10010 = 6.0
00011 = 21.8	10011 = 5.5
00100 = 20.0	10100 = 5.0
00101 = 18.4	10101 = 4.6
00110 = 17.1	10110 = 4.3
00111 = 16.0	10111 = 4.0
01000 = 15.0	11000 = 3.7
01001 = 13.3	11001 = 3.3
01010 = 12.0	11010 = 3.0
01011 = 10.9	11011 = 2.7
01100 = 10.0	11100 = 2.5
01101 = 9.2	11101 = 2.3
01110 = 8.6	11110 = 2.1
01111 = 8.0	11111 = 2.0

Delay Time:
00 = 250 ms
01 = 500 ms
10 = 750 ms
11 = 1000 ms

0 (Reserved)

ENABLE (F4h)

Sending the Enable command (F4h) to the keyboard starts its scanning function. After receiving this command, the keyboard returns an ACK (acknowledge) code, clears the output buffer, and starts scanning.

DISABLE (F5h)

The Disable command (F5h) halts keyboard scanning. After receiving this command, the keyboard returns an ACK (acknowledge) code to the system.

SET DEFAULT CONDITIONS (F6h)

The Set Default Conditions command (F6h) causes the keyboard to send an ACK code and its default conditions to the system. If the keyboard was enabled prior to receiving the Set Default Conditions command, the keyboard continues scanning.

NOP (F7h..FDh)

The keyboard responds to the NOP command with an ACK code. No other action is taken.

RESEND (FEh)

The Resend command (FEh) is issued to the keyboard only after a keyboard transmission. The keyboard responds by re-transmitting the most recent byte transmitted to the system.

RESET (FFh)

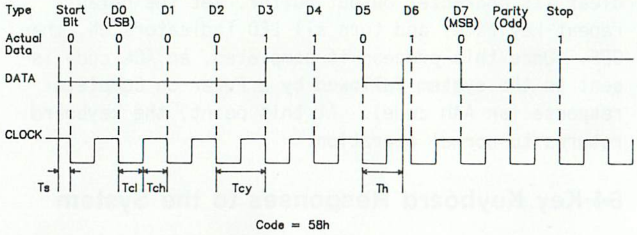
The Reset command (FFh) causes the keyboard to return an ACK code to the system. For the system to accept the ACK code, the system raises the clock and data lines for at least 500 ms. Upon receiving the Reset command, the keyboard is disabled until either the ACK code is accepted by the system or another command is issued to the keyboard.

If the Reset command is accepted, the keyboard will clear its character output buffer, set the default repeat-key rate, and turn all LED indicators ON, then OFF. Once this process is completed, an ACK code is sent to the system followed by a Power-on Complete response (an AAh code). At this point, the keyboard returns to normal operation.

84-Key Keyboard Responses to the System

Before the keyboard responses are sent to the system, the keyboard verifies the status of two signals, clock and data. Should the clock signal be low (0), the keyboard recognizes an inhibited state, and loads the keystrokes into its buffer. Once the inhibited state is removed, the keystrokes are sent to the system. If the data signal is low, the keyboard recognizes a REQUEST-TO-SEND condition from the system. Keystrokes are also loaded into the keyboard's buffer for this state and the keyboard prepares to receive the system commands. Once this state is cleared, the stored keystrokes are sent to the system.

The keyboard transmits keystrokes to the system only when both the clock and data signal are high (1). Data transmitted to the system consists of 11 bits: a start bit, 8 data bits, an odd parity bit, and a stop bit. Figure 5-7 shows the timing transmission for keyboard responses sent to the system.



Symbol	Parameter	Minimum	Maximum
Tcy	Cycle Time	60 us	80 us
Tcl	Clock Low	30 us	35 us
Tch	Clock High	30 us	45 us
Ts	Data Setup	8 us	14 us
Th	Data Hold	45 us	62 us

Note: CLOCK signal clamped low by system to inhibit keyboard.

Figure 5-7. Timing Diagram Standard for Keyboard-to-System Transmissions

The system can halt a keyboard transmission by setting the clock signal low. The keyboard checks the clock signal every 60 us to verify the signal's state. If the clock signal is detected as low, the keyboard will finish this transmission only if the rising edge of the clock pulse for the parity bit has not occurred.

Responses sent from the keyboard to the system are listed in Table 5-4.

Table 5-4. Keyboard Responses to the System

Code	Function
00h	Overrun
AAh	Power-Up Complete
EEh	Echo
F0h	Break
FAh	ACK
FEh	Resend

OVERRUN (00h)

The keyboard places 00h as the last character in the keyboard character buffer to indicate a buffer overrun.

POWER-UP COMPLETE (AAh)

The keyboard transmits the Power-up Complete response (AAh) to the system upon completion of power-on and removal of the keyboard inhibit state, or on receiving a Reset command from the system.

ECHO (EEh)

The keyboard transmits an Echo response to the system in response to the system's Echo command. This response is substituted for the ACK code.

BREAK (F0h)

When a key is released, the keyboard transmits a Break prefix (F0h), followed by the Make code for that particular key.

ACK (FAh)

The keyboard transmits an ACK code (FAh) in response to recognized system commands, except for an Echo or Resend command. If the system begins a transmission during an ACK code response, the keyboard discards this ACK code and the new system command is accepted and processed. If the command is not recognized, the keyboard sends a Resend command to the system.

RESEND (FEh)

The keyboard transmits a Resend response (FEh) to the system in response to an unknown system command. The Resend response instructs the system to retransmit its last command.

Enhanced Keyboard

The enhanced keyboard is capable of performing all the functions of the 84-key keyboard. It also supports a number of additional modes and functions. The most salient features are a separate cursor control key cluster and the addition of keys F11 and F12. For a layout of the keyboard and the position number assigned to each key, see Figure 5-8.

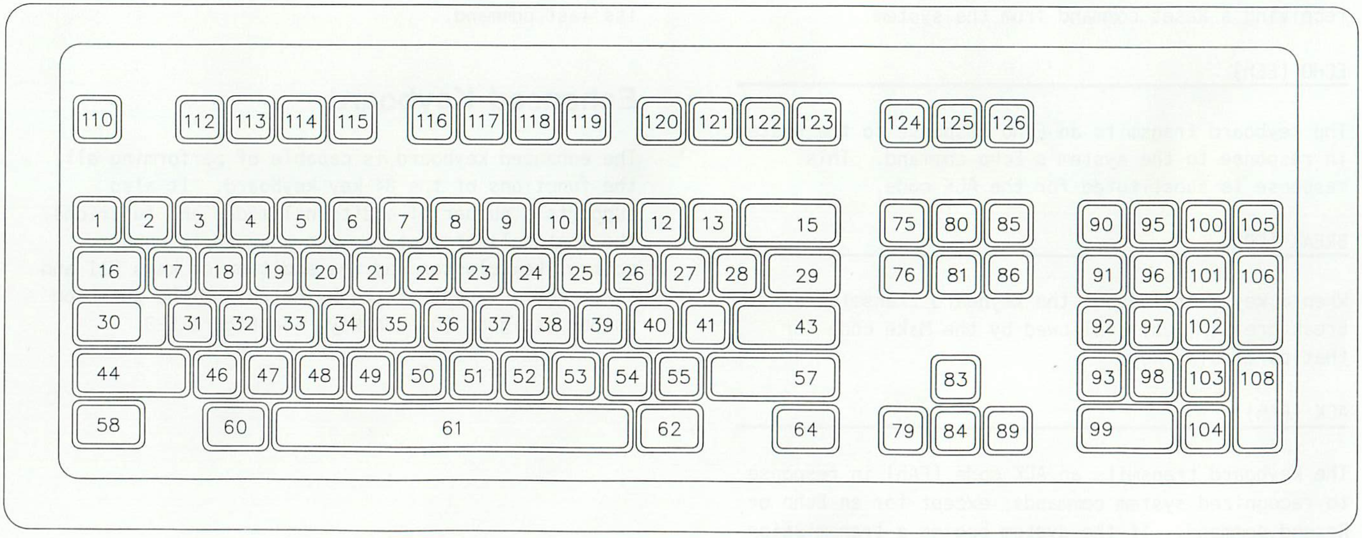


Figure 5-8. Assigned Position Number for Each Key on the Enhanced Keyboard

The enhanced keyboard has three operating modes. Each can be selected via keyboard commands, which are discussed in more detail later in this section. These modes offer a range of functionality and compatibility features to software applications.

Mode 1

In Mode 1, the scan codes generated by the enhanced keyboard are compatible with keyboards used in 8088 and 8086-based systems. To enter Mode 1, disable the scan code translation by the 8042 keyboard controller. The scan codes generated by Mode 1 of the keyboard are identical to system codes required for input to the BIOS. To operate in this mode, the F0h keyboard command should be sent, which explicitly selects Mode 1. To obtain system codes and status information, BIOS INT 16h functions AH-00h, 01h, and 02h should be used by applications operating the keyboard in Mode 1.

Mode 2

In Mode 2, the enhanced keyboard generates scan codes compatible with the 84-key keyboard. Mode 2 is the default mode of the enhanced keyboard that is selected by the COMPAQ DESKPRO 386 during power-on initialization. In this mode, the 8042 keyboard controller scan code translation is enabled so that the scan codes generated by the keyboard can be translated to the system codes required by the BIOS. Except for the system codes associated with the new keys of the enhanced keyboard, the system codes resemble the scan codes generated by the keyboard in Mode 1. In order to properly access the system codes generated by the new keys of the enhanced keyboard, applications should use BIOS functions INT 16h AH=10h, 11h, and 12h instead of the traditional functions INT 16h AH=00h, 01h, and 02h. During power-on, Num Lock is set active to enable the numeric keypad.

Mode 3

Mode 3 generates a different scan code set than Modes 1 or 2. In this mode, the 8042 keyboard controller translation must be disabled since the 8042 is not capable of translating the scan code set generated. Applications wishing to use the enhanced keyboard in Mode 3 should explicitly select this mode via the F0h keyboard command. These applications must assume responsibility for directly handling the scan codes generated by the keyboard since the 8042 and BIOS are not capable of handling the scan code set generated in Mode 3.

Tables 5-5, 5-6, 5-7, 5-8, and 5-9 show the scan code sets generated by the enhanced keyboard Modes 1, 2, and 3. For Mode 1, a Break code consists of a Make code with the high bit (bit 7) set to 1. For example, 9Ch is the Break code for 1Ch, and A0h is the Break code for 20h. For Modes 2 and 3, a Break code is a 2-byte sequence consisting of the Make code immediately preceded by the F0h. For example, F0h 0Eh is the Break code for 0Eh.

In Modes 2 and 3, the enhanced keyboard generates the Break codes by adding F0h to the Make code. In Mode 1, the enhanced keyboard generates the Break codes by setting to a 1 the most-significant bit of the Make code.

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
1	`	29	
2	1	02	
3	2	03	
4	3	04	
5	4	05	
6	5	06	
7	6	07	
8	7	08	
9	8	09	
10	9	0A	
11	0	0B	
12	-	0C	
13	+	0D	
15	Backspace	0E	
16	Tab	0F	
17	Q	10	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
18	W	11	
19	E	12	
20	R	13	
21	T	14	
22	Y	15	
23	U	16	
24	I	17	
25	O	18	
26	P	19	
27	[	1A	
28	]	1B	
29	/	2B	
30	Caps Lock	3A	
31	A	1E	
32	S	1F	
33	D	20	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
34	F	21	
35	G	22	
36	H	23	
37	J	24	
38	K	25	
39	L	26	
40	;	27	
41	"	28	
43	Enter	1C	
44	(Left) Shift	2A	
46	Z	2C	
47	X	2D	
48	C	2E	
49	V	2F	
50	B	30	
51	N	31	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
52	M	32	
53	,	33	
54	.	34	
55	/	35	
57	(Right) Shift	36	
58	Ctrl	1D	
60	(Left) Alt	38	
61	(Space Bar)	39	
62	(Right) Alt	E0 38	
64	(Right) Ctrl	E0 1D	
75	Ins	E0 52	3
76	Del	E0 53	3
79	(Left Arrow)	E0 4B	3
80	Home	E0 47	3
81	End	E0 4F	3
83	(Up Arrow)	E0 48	3

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
84	(Down Arrow)	E0 50	3
85	PgUp	E0 49	3
86	PgDn	E0 51	3
89	(Right Arrow)	E0 4D	3
90	Num Lock	45	4
91	7	47	4
92	4	4B	4
93	1	4F	4
95	/	E0 35	4
96	8	48	4
97	5	4C	4
98	2	50	4
99	0	52	4
100	*	37	4
101	9	49	4
102	6	4D	4

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
103	3	51	4
104	.	53	4
105	-	4A	4
106	+	4E	4
108	Enter	E0 1C	4
110	Esc	01	
112	F1	3B	
113	F2	3C	
114	F3	3D	
115	F4	3E	
116	F5	3F	
117	F6	40	
118	F7	41	
119	F8	42	
120	F9	43	
121	F10	44	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-5. Keyboard Scan Codes for Mode 1 (Concluded)

Key Location	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Notes
122	F11	57	
123	F12	58	
124	Print Screen	E0 2A E0 37	
125	Scroll Lock	46	
126	Pause	E1 1D 45 E1 9D C5	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. System code refers to the code input to the BIOS. Note that in Mode 1, the system codes are identical to the scan codes, because no translation is performed by the 8042 keyboard controller.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

The following keys have special codes during Mode 1 operation depending on the state of the Shift, Num Lock, Alt, and Ctrl keys. Table 5-6 shows the scan codes generated by these keys.

Table 5-6. Combination Scan Codes for Mode 1

Key Location	Key Legend	Scan Code
Shift Active with Num Lock OFF:		
75	Ins	E0 AA E0 52
76	Del	E0 AA E0 53
79	(Left Arrow)	E0 AA E0 4B
80	Home	E0 AA E0 47
81	End	E0 AA E0 4F
83	(Up Arrow)	E0 AA E0 48
84	(Down Arrow)	E0 AA E0 50
85	PgUp	E0 AA E0 49
86	PgDn	E0 AA E0 51
89	(Right Arrow)	E0 AA E0 4D
Shift Active with Num Lock ON:		
75	Ins	E0 2A E0 52
76	Del	E0 2A E0 53
79	(Left Arrow)	E0 2A E0 4B
80	Home	E0 2A E0 47
81	End	E0 2A E0 4F
83	(Up Arrow)	E0 2A E0 48
84	(Down Arrow)	E0 2A E0 50
85	PgUp	E0 2A E0 49
86	PgDn	E0 2A E0 51
89	(Right Arrow)	E0 2A E0 4D

(Continued)

Table 5-6. Combination Scan Codes for Mode 1 (Concluded)

Key Location	Key Legend	Scan Code
Shift Active with Num Lock OFF:		
95	Keypad /	E0 AA E0 35
Shift Active or Ctrl Active:		
124	Print Screen	E0 37 / E0 B7
Alt Active:		
124	Print Screen	54 / D4
Ctrl Active:		
126	Pause	E0 46 E0 C6

Note: Key 126 is not typematic and generates a scan code only on the Make condition.

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
1	`	0E	29	
2	1	16	02	
3	2	1E	03	
4	3	26	04	
5	4	25	05	
6	5	2E	06	
7	6	36	07	
8	7	3D	08	
9	8	3E	09	
10	9	46	0A	
11	0	45	0B	
12	-	4E	0C	
13	+	55	0D	
15	Backspace	66	0E	
16	Tab	0D	0F	
17	Q	15	10	
18	W	1D	11	
19	E	24	12	
20	R	2D	13	
21	T	2C	14	
22	Y	35	15	
23	U	3C	16	
24	I	43	17	
25	O	44	18	
26	P	4D	19	
27	[	54	1A	
28	]	5B	1B	
29	/	5D	2B	
30	Caps Lock	58	3A	
31	A	1C	1E	
32	S	1B	1F	
33	D	23	20	
34	F	2B	21	
35	G	34	22	
36	H	33	23	
37	J	3B	24	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
38	K	42	25	
39	L	4B	26	
40	;	4C	27	
41	"	52	28	
43	Enter	5A	1C	
44	(Left) Shift	12	2A	
46	Z	1A	2C	
47	X	22	2D	
48	C	21	2E	
49	V	2A	2F	
50	B	32	30	
51	N	31	31	
52	M	3A	32	
53	,	41	33	
54	.	49	34	
55	/	4A	35	
57	(Right) Shift	59	36	
58	(Left) Ctrl	14	1D	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

Continued)

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	System Code (hex)	Note
60	(Left) Alt	11	38	
61	(Space)	29	39	
62	(Right) Alt	E0 11	E0 38	
64	(Right) Ctrl	E0 14	E0 1D	
75	Ins	E0 70	E0 52	3
76	Del	E0 71	E0 53	3
79	(Left Arrow)	E0 6B	E0 4B	3
80	Home	E0 6C	E0 47	3
81	End	E0 69	E0 4F	3
83	(Up Arrow)	E0 75	E0 48	3
84	(Down Arrow)	E0 72	E0 50	3
85	PgUp	E0 7D	E0 49	3
86	PgDn	E0 7A	E0 51	3
89	(Right Arrow)	E0 74	E0 4D	3
90	Num Lock	77	45	4
91	7	6C	47	4
92	4	6B	4B	4
93	1	69	4F	4

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
95	/	E0 4A	E0 35	4
96	8	75	48	4
97	5	73	4C	4
98	2	72	50	4
99	0	70	52	4
100	*	7C	37	4
101	9	7D	49	4
102	6	74	4D	4
103	3	7A	51	4
104	.	71	53	4
105	-	7B	4A	4
106	+	79	4E	4
108	Enter	E0 5A	E0 1C	4
110	Esc	76	01	
112	F1	05	3B	
113	F2	06	3C	
114	F3	04	3D	
115	F4	0C	3E	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

(Continued)

Table 5-7. Keyboard Scan Codes for Enhanced Keyboard Mode 2 (Concluded)

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	System Code (hex)	Note
116	F5	03	3F	
117	F6	0B	40	
118	F7	83	41	
119	F8	0A	42	
120	F9	01	43	
121	F10	09	44	
122	F11	78	57	
123	F12	07	58	
124	Print Screen	E0 12 E0 7C	E0 2A E0 37	
125	Scroll Lock	7E	46	
126	Pause	E1 14 77 E1 F0 14 F0 77	E1 1D 45 E1 9D C5	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. The system code is the code as translated by the 8042 keyboard controller and input to the BIOS.
2 All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. Scan codes listed are for Num Lock inactive.
4. This is a numeric cluster key.

The following keys have special codes during Mode 2 operation depending on the state of the Shift, Num Lock, Alt, and Ctrl keys. Table 5-8 shows the scan codes generated by these keys.

Table 5-8. Combination Scan Codes for Mode 2

Key Location	Key Legend	Scan Code
Shift Active with Num Lock OFF:		
75	Ins	E0 F0 12 E0 70
76	Del	E0 F0 12 E0 71
79	(Left Arrow)	E0 F0 12 E0 6B
80	Home	E0 F0 12 E0 6C
81	End	E0 F0 12 E0 69
83	(Up Arrow)	E0 F0 12 E0 75
84	(Down Arrow)	E0 F0 12 E0 72
85	PgUp	E0 F0 12 E0 7D
86	PgDn	E0 F0 12 E0 7A
89	(Right Arrow)	E0 F0 12 E0 74
Shift Inactive with Num Lock ON:		
75	Ins	E0 12 E0 70
76	Del	E0 12 E0 71
79	(Left Arrow)	E0 12 E0 6B
80	Home	E0 12 E0 6C
81	End	E0 12 E0 69
83	(Up Arrow)	E0 12 E0 75
84	(Down Arrow)	E0 12 E0 72
85	PgUp	E0 12 E0 7D
86	PgDn	E0 12 E0 7A
89	(Right Arrow)	E0 12 E0 74
Shift Active with Num Lock OFF:		
95	Keypad /	E0 F0 12 4A

(Continued)

Table 5-8. Combination Scan Codes for Mode 2 (Concluded)

Key Location	Key Legend	Scan Code
Shift Active or Ctrl Active:		
124	Print Screen	E0 7C
Alt Active:		
124	Print Screen	84
Ctrl Active:		
126	Pause	E0 7E E0 F0 7E

Note: Key 126 is not a repeat key and generates a scan code only on the Make condition.

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1, 2)	Note
1		0E	
2	1	16	
3	2	1E	
4	3	26	
5	4	25	
6	5	2E	
7	6	36	
8	7	3D	
9	8	3E	
10	9	46	
11	0	45	
12	-	4E	
13	+	55	
15	Backspace	66	
16	Tab	0D	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Note
17	Q	15	
18	W	1D	
19	E	24	
20	R	2D	
21	T	2C	
22	Y	35	
23	U	3C	
24	I	43	
25	O	44	
26	P	4D	
27	[	54	
28	]	5B	
29	/	5C	
30	Caps Lock	14	
31	A	1C	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Note
32	S	1B	
33	D	23	
34	F	2B	
35	G	34	
36	H	33	
37	J	3B	
38	K	42	
39	L	4B	
40	;	4C	
41	"	52	
43	Enter	5A	
44	(Left) Shift	12	
46	Z	1A	
47	X	22	
48	C	21	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Note
49	V	2A	
50	B	32	
51	N	31	
52	M	3A	
53	,	41	
54	.	49	
55	/	4A	
57	(Right) Shift	59	
58	(Left) Ctrl	11	
60	(Left) Alt	19	
61	(Space Bar)	29	
62	(Right) Alt	39	
64	(Right) Ctrl	58	
75	Ins	67	
76	Del	64	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Notes
79	(Left Arrow)	61	
80	Home	6E	
81	End	65	
83	(Up Arrow)	63	
84	(Down Arrow)	60	
85	PgUp	6F	
86	PgDn	6D	
89	(Right Arrow)	6A	
90	Num Lock	76	3
91	7	6C	3
92	4	6B	3
93	1	69	3
95	/	77	3
96	8	75	3
97	5	73	3

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Notes
98	2	72	3
99	0	70	3
100	*	7E	3
101	9	7D	3
102	6	74	3
103	3	7A	3
104	.	71	3
105	-	84	3
106	+	7C	3
108	Enter	79	3
110	Esc	08	
112	F1	07	
113	F2	0F	
114	F3	17	
115	F4	1F	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

(Continued)

Table 5-9. Scan Codes for Enhanced Keyboard Mode 3 (Concluded)

Key Code	Key Cap Legend	Scan Code (hex) (Notes 1 & 2)	Notes
116	F5	27	
117	F6	2F	
118	F7	37	
119	F8	3F	
120	F9	47	
121	F10	4F	
122	F11	56	
123	F12	5E	
124	Print Screen	57	
125	Scroll Lock	5F	
126	Pause	62	

Notes:
1. Scan code refers to the code generated by the keyboard when a key is pressed. No system code is shown in this mode, because in keyboard Mode 3 the 8042 keyboard controller scan code translation should be disabled. The application should directly handle all scan codes as generated by the keyboard.
2. All scan codes listed are for Shift, Alt, and Ctrl inactive.
3. This is a numeric cluster key.

In addition to the commands supported by the 84-key keyboard, the enhanced keyboard supports a number of commands related to its enhanced programmable functions. Table 5-10 shows the additional commands supported by the enhanced keyboard.

Table 5-10. Additional Commands Supported by Enhanced Keyboard

Command Code	Function
F2h	This is the command code that requests the identification sequence from the keyboard. The keyboard should respond with an ACK and the 2-byte identification code. The enhanced keyboard identification sequence is ABh followed by 83h. The keyboard scanning is then enabled.
EFh, F1h	The enhanced keyboard does not acknowledge these commands. The keyboard transmits a Resend response and continues scanning for keys.
F0h	Selects one of three modes of operation for the enhanced keyboard. This is a 2-byte command sequence. The second byte specifies the mode of the enhanced keyboard. The second byte is as follows: 01 - Selects Mode 1 of the keyboard. 02 - Selects Mode 2 of the keyboard. 03 - Selects Mode 3 of the keyboard.
F7h	Programs all keys to be able to perform the repeat function. This command is only enabled during Mode 3 keyboard operation.
F8h	Programs all keys to generate Make/Break codes. This command is only enabled during Mode 3 keyboard operation.
F9h	Programs all keys to generate only Make codes. This command is only enabled during Mode 3 keyboard operation.
FAh	Programs all keys for Make/Break and repeat operations. This command is only enabled during Mode 3 keyboard operation.
FBh	This is a 2-byte command to enable the repeat function of an individual key. The second byte of the command is the Make code that identifies the key to be affected by the command. This command is only enabled during Mode 3 keyboard operation. Keyboard scanning is disabled after this command.

(Continued)

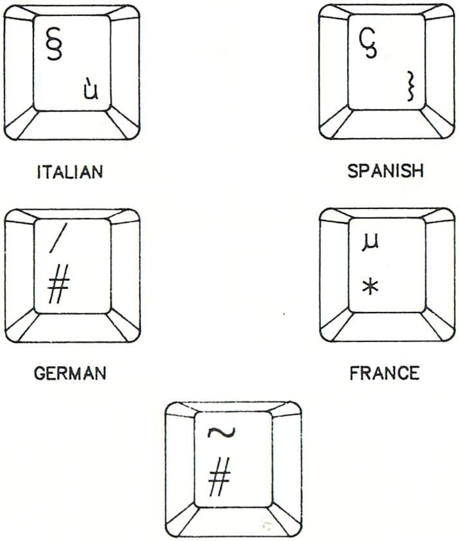
Table 5-10. Additional Commands Supported by Enhanced Keyboard (Concluded)

Command Code	Function
FCh	This is a 2-byte command to program an individual key to generate Make and Break codes. The second byte of the command is the Make code that identifies the key to be affected by the command. This command is only enabled during Mode 3 keyboard operation. Keyboard scanning is disabled after this command.
FDh	This is a 2-byte command to program an individual key to generate only Make codes. The second byte of the command is the Make code that identifies the key to be affected by the command. This command is only enabled during Mode 3 keyboard operation. Keyboard scanning is disabled after this command.

Figure 5-8 shows the key legends associated with key 42 for the international enhanced keyboards. Figure 5-9 shows the legends for key 45. Table 5-11 lists the scan codes for these keys.

Table 5-11. International Scan Codes

Keycode	Mode 1 Scan Code (h)	Mode 2 Scan Code (h)	Mode 3 Scan Code (h)
42	2B	5D	53
45	56	61	13

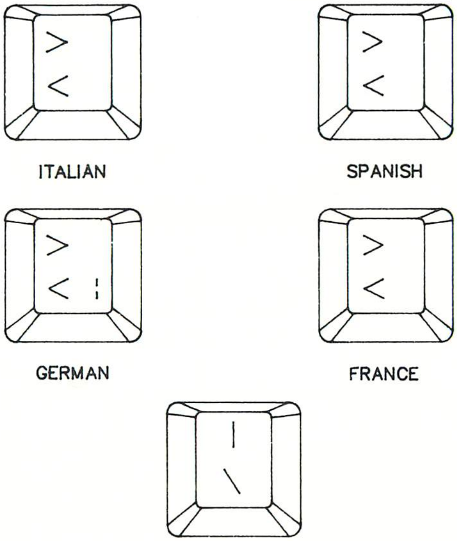


ITALIAN SPANISH

GERMAN FRANCE

UK

Figure 5-9. Key 42



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GERMAN FRANCE

UK

Figure 5-10. Key 45

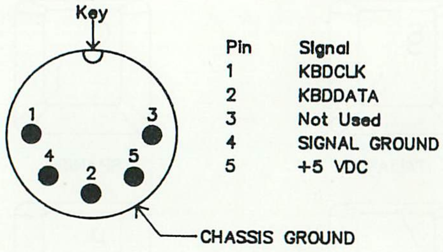
5.5 CONNECTORS

The keyboard for the COMPAQ DESKPRO 386 uses a 6-pin modular-type connector, which is shown in Figure 5-11. Table 5-12 lists the keyboard connector signals.

Table 5-12. Keyboard Cable Connector Signals

COMPAQ DESKPRO 386 Pin	Signal
1	KBCLK (Keyboard Clock Signal)
2	KBDATA (Keyboard Data Signal)
3	Reserved
4	Signal Ground
5	Power (See Note)
Shield	Chassis Ground

Note: Power for the COMPAQ DESKPRO 386 is +5 VDC.



Pin	Signal
1	KBDCLK
2	KBDDATA
3	Not Used
4	SIGNAL GROUND
5	+5 VDC

Figure 5-11. COMPAQ DESKPRO 386 Keyboard Connector

Chapter 6
POWER SUPPLY

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POWER SUPPLY

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Chapter 6
POWER SUPPLY

6.1 INTRODUCTION

The COMPAQ DESKPRO 386 system uses a switching-type power supply to provide high-amperage, low-noise, direct current (DC) power for the system. The COMPAQ DESKPRO 386 power supply was designed to complement the other enhancements of the system by providing 192 watts (w) of steady-state power.

The power supply provides four voltage levels for the system: +5 VDC, -5 VDC, +12 VDC, and -12 VDC. To provide good power regulation, the +12 VDC is provided as two separate outputs: main and auxiliary.

AC Input

The power supply alternating-current (AC) input is factory-selectable to 120 VAC (domestic) or 220 to 240 VAC (international). The power supply has different alternating-current power fuses for the domestic and international versions.

Note: Only Authorized COMPAQ Service Representatives should change the alternating-current input configuration. Changing the alternating-current input configuration invalidates the COMPAQ warranty. The label near the alternating-current power switch states the alternating-current input power requirements for your system.

Model Configuration Limitation

If a second 40-MB fixed disk drive is added to a Model 40 COMPAQ DESKPRO 386, a 40-MB fixed disk drive back-up cannot be added.

Power-On Sequence

The power-on sequence guarantees that all outputs are above the specified low-voltage limits within 100 ms of power-on. The output load determines the order and the amount of time after the PWRGOOD signal is active (high) in which the outputs reach their regulated voltage level. Signal +5VRST is also set high at or prior to PWRGOOD becoming active (high).

Power-Down Sequence

The power-down sequence is dependent on the same variables as the power-on sequence. The output load determines both the order in which the output voltages drop out of regulation and the time remaining after the PWRGOOD signal becomes inactive (low). The PWRGOOD signal goes low within 8 ms after the power switch is turned off.

Autocycle Circuitry

The autocycle circuitry is the heart of the fault-detection functions for the power supply. When a fault is detected, the autocycle circuitry causes the power supply to shut off for approximately 2 seconds, then allows it to try to start up. If the fault still exists, the power supply stays off for another 2 seconds, then again tries to start up. This is a continuing process.

The following paragraphs describe the fault-detection circuits that trigger the autocycle circuitry for system protection.

The overvoltage protection circuit provides two types of protection. First, all outputs have a zener diode that shorts to ground any supply voltage that exceeds specifications. Second, the +5 VDC output has an overvoltage crowbar circuit that triggers the autocycle function when the output exceeds 5.6 VDC.

The low-voltage protection circuit monitors the direct-current outputs. When one of the outputs drops below the specified limit, it triggers the autocycle circuit.

The alternating-current input overcurrent protection circuit is a fuse on the outside of the unit. The fuse rating varies with the model. A spare fuse is included in the fuse-holder assembly.

The brownout-protection circuit and the autocycle circuit are triggered if the alternating-current input voltage drops to 65-100 VAC (domestic) or 130-200 VAC (international) under nominal to heavy loads.

CAUTION

Do not attempt to disassemble or repair the power supply. It has no user-serviceable components. Never operate the power supply without a load.

6.2 SPECIFICATIONS

Tables 6-1 through 6-3 provide the power supply specifications.

Table 6-1. Power Supply Specifications

Input AC voltage RMS:	
Domestic	102 to 132 VAC
International	204 to 264 VAC
Line frequency	47 to 62 Hz
Input fuse rating:	
120 VAC RMS	5 A
220-240 VAC RMS	2.5 A
In-rush current (peak, over one line cycle interval):	
120 VAC	40 A
220-240 VAC	80 A
Environment:	
Temperature	41°F to 113°F (5°C to 45°C)
Altitude	0 to 10,000 ft (0 to 3000 m)
Relative humidity	5% to 95%

(Continued)

Table 6-1. Power Supply Specifications (Concluded)

Power dissipation (Note 1):	
Starting (Note 2)	220 w
Steady state	192 w

	Current (In Amperes)				
Voltage Regulation:	Nominal	Min.	Max.	Abs. Max. (Note 3):	Variance
+5 VDC	+ 5.0	1.5	20.0		(±2%)
+12 VDC	+12.25	1.0	5.0	7.0	(±2%)
+12 VDC(Aux)	+12.25	0.0	5.0	7.0	(±2%)
-5 VDC	-5.0	0.0	0.5		(±5%)
-12 VDC	-12.0	0.0	1.0		(±5%)

Over-Voltage Limits:	
+5 VDC	5.6 VDC
+12 VDC	13.0 VDC
-5 VDC	-5.6 VDC
-12 VDC	-13.0 VDC
Maximum Ripple/Output	50 mV RMS

Notes:
1. These limits were established under the following conditions: 120 V, 60 Hz, 25°C, mean sea level, and 50-percent relative humidity.
2. Peak output power may be used on a 5-percent duty cycle, not to exceed 30 seconds of continuous operation.
3. Abs. Max. = absolute maximum current. The peak output power may be used on a 5-percent duty cycle, not to exceed 30 seconds of continuous operation.

Table 6-2 gives the amounts of power available for typical COMPAQ DESKPRO 386 configurations. It also gives the remaining amounts of power available for use by expansion boards. Note that the amount of power drawn from each expansion slot is limited to that given in Table 6-3. Limitations of the +12 VDC supply do not allow the installation of two 40-MB fixed disk drives and a fixed disk drive back-up in the same unit.

Table 6-2. Power Allocation per Slot (In Amperes)

Slot	+5 VDC	+12 VDC	-12 VDC	-5 VDC
8-Bit	3.0	1.5	1.5	1.5
16-Bit	4.5	1.5	1.5	1.5

Table 6-3 lists the power available for expansion in a typical COMPAQ DESKPRO 386 with the following configurations:

- System board
- System memory board (1 MB)
- Multipurpose Fixed Disk Controller Board
- COMPAQ Enhanced Color Graphics Board
- 1.2-MB Diskette Drive
- 40-MB Fixed Disk Drive
- 40-MB Fixed Disk Drive Back-up
- 84-Key Keyboard

Table 6-3. COMPAQ DESKPRO 386 Power Available for Expansion

	Total Power Available (In Amperes)			
Typical Configuration	+5VDC	+12VDC	-12VDC	-5VDC
With Dual-Mode Monitor	8.0	2.0	0.3	0.2
With Color Monitor	8.0	3.5	0.3	0.2

6.3 CONNECTORS

Table 6-4 describes the DESKPRO 386 power supply signals. Figure 6-1 shows the voltages or signals provided by the power supply to the system board.

Table 6-4. Power Supply Connector to the System Board

Signal	Pin	I/O	Description
+5VRST	1	0	The +5VRST signal is regulated from the +15 VDC line. This signal ranges from +4.8 VDC to +5.2 VDC.
PWRGOOD	2	0	The PWRGOOD signal is controlled by the low-voltage monitor and the missing cycle detector circuits. When all outputs are above the minimum values (see specifications), and there is no fault, the PWRGOOD signal is TTL high (+3.5 to +5.25 VDC). If a low-voltage condition is detected, the PWRGOOD signal is pulled low (less than 0.4 VDC).
+5 VDC	11,12,13	0	+5.0 VDC
+5VS	14	I	The +5VS signal provides feedback from the system board. The power supply shuts down when the +5VS signal is interrupted or disconnected.
Ground	6,7,8,9,19,20		Signal Ground
-5 VDC	10	0	-5 VDC
-12 VDC	5	0	-12 VDC
+12VMAIN	15,18	0	+12 VDC for J111 and J112 (diskette drives A and B) and expansion bus slots
+12VAUX	16,17	0	+12 VDC for J109 and J110 (fixed disk drive C and fixed disk drive back-up) and J113 (COMPAQ Dual-Mode Monitor power)
No Connection	3,4	- -	- -

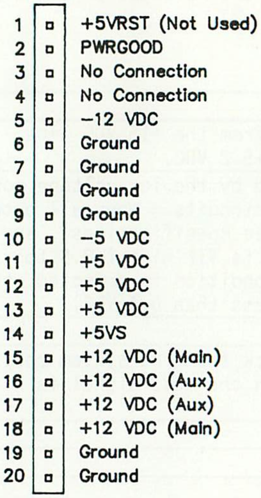

Figure 6-1. COMPAQ DESKPRO 386 Power Supply Cable Pinout

OPTIONS

Chapter 7
MULTIPURPOSE FIXED DISK CONTROLLER BOARD

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MULTIPURPOSE FIXED DISK CONTROLLER

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Chapter 7
MULTIPURPOSE FIXED DISK CONTROLLER

7.1 INTRODUCTION

The Multipurpose Fixed Disk Controller supplies diskette drive functions, serial asynchronous communications functions, and parallel printer communications functions. It also controls the 40-MB fixed disk drive back-up.

The Multipurpose Fixed Disk Controller also interfaces with the 40-MB fixed disk drive. This drive has an integrated controller on the logic board that is attached to the drive. The Multipurpose Fixed Disk Controller circuitry provides address decoding, buffers, and control and data connectors for the fixed disk drive controller.

Note: If a second 40-MB fixed disk drive is added to a Model 40 COMPAQ DESKPRO 386, a 40-MB fixed disk drive back-up cannot be added.

Figure 7-1 shows the component layout for the controller. Figure 7-2 shows the functional block diagram of the multipurpose controller.

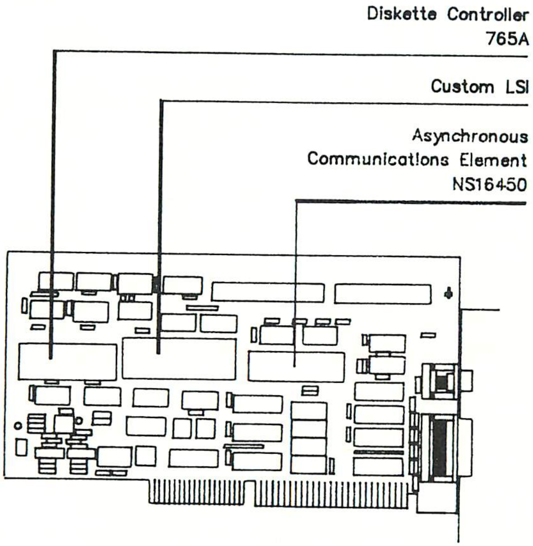


Figure 7-1. Multipurpose Fixed Disk Controller Component Layout

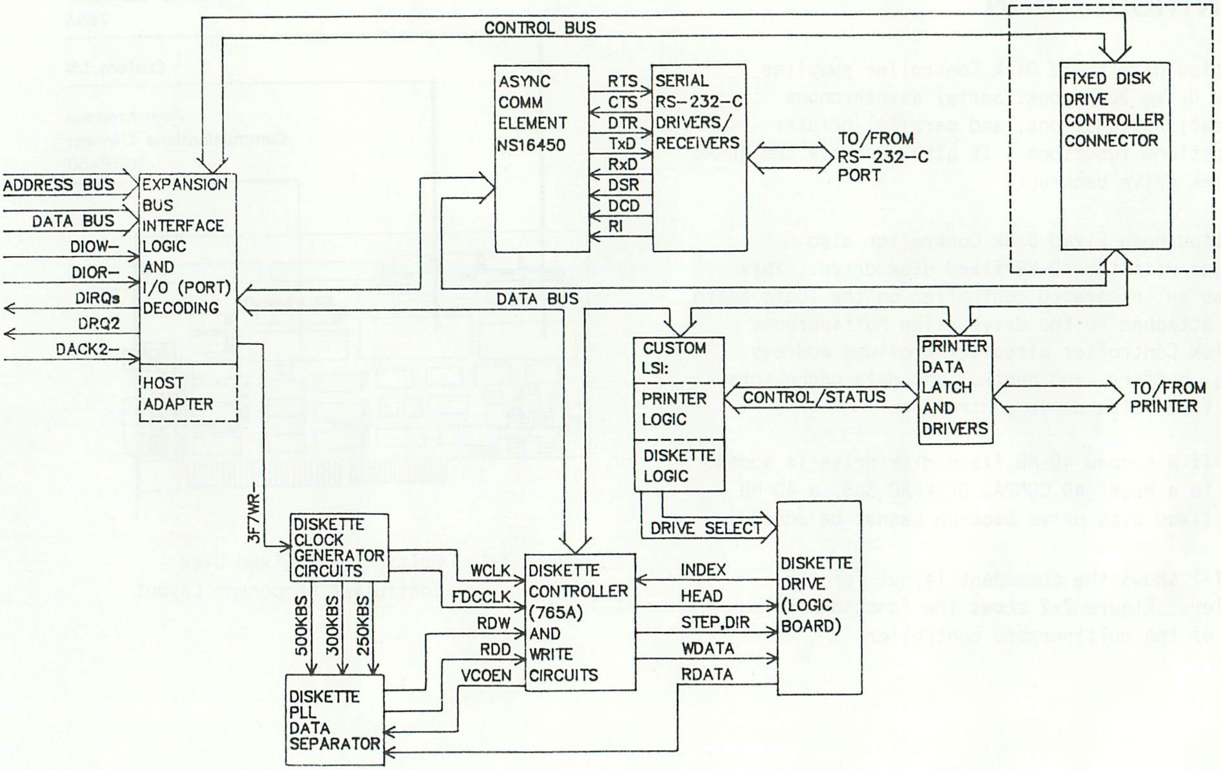

CONTROL BUS
ASYNC COMM ELEMENT NS16450
RTS
CTS
DTR
TxD
RxD
DSR
DCD
RI
SERIAL RS-232-C DRIVERS/ RECEIVERS
TO/FROM RS-232-C PORT
FIXED DISK DRIVE CONTROLLER CONNECTOR
ADDRESS BUS
DATA BUS
DIOW-
DIOR-
DIRQs
DRQ2
DACK2-
EXPANSION BUS INTERFACE LOGIC AND I/O (PORT) DECODING
HOST ADAPTER
DATA BUS
CUSTOM LSI:
PRINTER LOGIC
DISKETTE LOGIC
CONTROL/STATUS
PRINTER DATA LATCH AND DRIVERS
TO/FROM PRINTER
3F7WR-
DISKETTE CLOCK GENERATOR CIRCUITS
500KBS
300KBS
250KBS
WCLK
FDCCLK
RDW
RDD
VCOEN
DISKETTE CONTROLLER (765A) AND WRITE CIRCUITS
INDEX
HEAD
STEP,DIR
WDATA
RDATA
DRIVE SELECT
DISKETTE DRIVE (LOGIC BOARD)
DISKETTE PLL DATA SEPARATOR

Figure 7-2. Multipurpose Fixed Disk Controller Functional Block Diagram

Three functions are controlled by programmable devices:

- Diskette controller functions are handled by a 765 disk controller.
- Asynchronous serial communications are handled by a NS16450.
- Parallel printer output and status are handled by a custom LSI device. The custom LSI device also handles some drive control functions and performs address decoding for the fixed disk drive controller interface.

The following sections describe these programmable devices and other multipurpose controller functions.

Table 7-1 shows the I/O ports used on the Multipurpose Fixed Disk Controller.

Table 7-1. Multipurpose Fixed Disk Controller I/O Ports

Port	R/W	Register Functions	Jumper Setting
2F8h	R/W	COM2 Divisor Latch LSB (with DLA bit = 1 (Note 1)	(J1, Position 2)
2F8h	R	COM2 Received Data (with DLA bit = 0 (Note 1)	"
2F8h	W	COM2 Transmit Data (with DLA bit = 0 (Note 1))	"
2F9h	R/W	COM2 Divisor Latch MSB (with DLA bit = 1 (Note 1)	"
2F9h	R/W	COM2 Interrupt Enable (with DLA bit = 0 (Note 1))	"
2FAh	R	COM2 Interrupt ID	"
2FAh	W	COM2 Reserved	"
2FBh	R/W	COM2 Line Control	"
2FCh	R/W	COM2 Modem Control	"
2FDh	R	COM2 Line Status	"
2FEh	R	COM2 Modem Status	"
2FFh	R/W	COM2 Scratch	"
370h	R/W	Diskette2 Reserved (Note 2)	(J2, Position 2)
371h	R/W	Diskette2 Reserved (Note 2)	"
372h	W	Diskette2 Drive Control (Note 2)	"
372h	R	Diskette2 Reserved (Note 2)	"
373h	R/W	Diskette2 Reserved (Note 2)	"

Notes:
1. The DLA bit is in the Line Control Register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.
2. Diskette1 and Diskette2 are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

(Continued)

Table 7-1. Multipurpose Fixed Disk Controller I/O Ports

Port	R/W	Register Functions	Jumper Setting
374h	R	Diskette2 Main Status (Note 2)	(J2, Position 2)
374h	W	Diskette2 Reserved (Note 2)	"
375h	R/W	Diskette2 Data (Note 2)	"
377h	R	Diskette2 and Fixed Disk 2 Status (Note 2)	"
377h	W	Diskette2 Data Rate (Note 2)	"
3BCh	R/W	Printer1 Data	SW2 ON
3BDh	R	Printer1 Status	"
3BDh	W	Printer1 Reserved	"
3BEh	R/W	Printer1 Control	"
3BFh	R/W	Printer1 Reserved	"
3F0h	R/W	Diskette1 Reserved	(J2, Position 1)
3F1h	R/W	Diskette1 Reserved	"
3F2h	W	Diskette1 Drive Control	"
3F2h	R	Diskette1 Reserved	"
3F3h	R/W	Diskette1 Reserved	"
3F4h	R	Diskette1 Main Status	"
3F4h	W	Diskette1 Reserved	"
3F5h	R/W	Diskette1 Data	"
3F7h	R	Diskette1 and Fixed Disk 1 Status	"
3F7h	W	Diskette1 Data Rate	"

Notes:
1. The DLA bit is in the Line Control Register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.
2. Diskette1 and Diskette2 are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

(Continued)

Table 7-1. Multipurpose Fixed Disk Controller I/O Ports (Concluded)

Port	R/W	Register Functions	Jumper Setting
3F8h	R/W	COM1 Divisor Latch LSB (with DLA bit = 1 (Note 1))	(J1, Position 1)
3F8h	R	COM1 Received Data (with DLA bit = 0 (Note 1))	"
3F8h	W	COM1 Transmit Data (with DLA bit = 0 (Note 1))	"
3F9h	R/W	COM1 Divisor Latch MSB (with DLA bit = 1 (Note 1))	"
3F9h	R/W	COM1 Interrupt Enable (with DLA bit = 0 (Note 1))	"
3FAh	R	COM1 Interrupt ID	"
3FAh	W	COM1 Reserved	"
3FBh	R/W	COM1 Line Control	"
3FCh	R/W	COM1 Modem Control	"
3FDh	R	COM1 Line Status	"
3FEh	R	COM1 Modem Status	"
3FFh	R/W	COM1 Reserved	"

Notes:
1. The DLA bit is in the Line Control Register. This bit must be set (=1) to access the divisor latches and reset (=0) to access the Data and the Interrupt Enable registers.
2. Diskette1 and Diskette2 are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

7.2 MULTIPURPOSE CONTROLLER CIRCUITS

The drive controller circuits control one or two 1.2-MB or 360-KB diskette drives, and a 40-MB fixed disk drive back-up.

The Multipurpose Fixed Disk Controller uses four I/O port addresses to transmit data to and from a diskette drive, to control the drive functions, and to read the current drive status. Table 7-2 lists the port addresses for the multipurpose controller.

Table 7-2. Multipurpose Fixed Disk Controller Port Addresses

Port 1	 2	R/W	Register Function
3F2h	372h	W	Drive Control
3F4h	374h	R	Drive Status
3F5h	375h	R/W	Data
3F7h	377h	W	Data Transfer Rate Control

The following sections describe the drive controller circuit functions:

- Drive Controller (765)
- Custom LSI Device
- Programmable Data Transfer Rate
- Data Separator
- Write Precompensation and Write Control

DRIVE CONTROL (3F2h, WRITE ONLY)

The Drive Control register is part of the Custom LSI device. It controls functions such as interrupt and DMA Enable, Drive MOTOR ON, DRIVE SELECT, and Controller Reset. The format for this register is:

```
   BIT
76543210
|||||||||
||||||└┴── 00 = Diskette drive 1 selected
||||||     01 = Diskette drive 2 selected
||||||     10 = Reserved
||||||     11 = Tape drive selected
|||||
|||||└─── 0 = Reset drive controller
||||      1 = Reenables drive controler
||||└──── 0 = Interrupts and DMA disabled
|||       1 = Interrupts and DMA enabled
|||
|||└───── 0 = Diskette drive 1 motor off
||        1 = Diskette drive 1 motor on
||
||└────── 0 = Diskette drive 2 motor off
|         1 = Diskette drive 2 motor on
|
└┴─────── 00 (Reserved)
```

MAIN STATUS (3F4h, READ ONLY)

The Main Status register is part of the 765 controller and is used as the Diskette Status register.

DATA (3F5h)

The Data register is part of the 765 drive controller. Data and 765 controller commands are written to the controller and data and status bytes are read from the controller through this port.

DATA TRANSFER RATE CONTROL (3F7h, WRITE ONLY)

This register contains the current data transfer rate in kilobits per second (kb/s). The format for this register is:

```
      BIT
76543210
||||||└┴── 00 = 500 kb/s
||||||     01 = 300 kb/s
||||||     10 = 250 kb/s
||||||     11 = Reserved
||||||
└┴┴┴┴┴──── 000000 (Reserved)
```

Drive Controller (765)

The 765 drive controller accepts commands from the system and controls most drive functions and the transfer of data to the drives.

The 765 operates in the DMA mode for data transfers to the system. It issues a DMA request signal (DRQ2) and receives a DMA acknowledge signal (DACK2-) for each byte transferred.

The 765 has two registers, a Data register and the Main Status register, as listed in Table 7-3. The Data register is used to program the device or to transmit or receive blocks of data.

Table 7-3. 765 Registers

Port 1	 2	Function
3F4h	374h	Main Status register
3F5h	375h	Data register

All 765 commands have three operating phases:

- The command phase, in which the 765 receives the command from the system.
- The execution phase, in which the 765 carries out the command.
- The results phase, in which the status and results are read back from the 765 to the system.

For detailed command information, refer to the 765 or Intel 8272A component data sheets.

Custom LSI Device

The custom LSI device is a circuit for address decoding and control signal timing. It is addressed as a port device to control the diskette drive motors and drive selection.

Programmable Data Transfer Rate

The system can transfer data with the diskette drives at 250, 300, or 500 kb/s. Table 7-4 lists the data transfer rates used by various drives. The Data Transfer Rate Control register (3F7h) describes the bits that specify the transfer rate.

Table 7-4. Programmable Data Transfer Rate

Transfer Rate (In Kilobits/Second)	When Used
500	1.2-MB diskette drive data
500	40-MB fixed disk drive back-up data
300	1.2-MB diskette drive data
250	Double-density diskette drive

Data Separator

Data separation is the process of separating the combined data and clock signal from the drives into separate clock and data lines. Several devices form a voltage-controlled oscillator/phase-locked loop arrangement to perform the data separation.

Write Precompensation

Write precompensation is a process of adding or removing small amounts of time between the pulses written to the disks. This process increases the data integrity at high data densities. The data density increases as the diskette drive head approaches the center tracks.

Write precompensation is always on. The amount of precompensation varies with the data transfer rate as given in Table 7-5.

Table 7-5. Write Precompensation Amounts

Transfer Rate (In Kilobits/Second)	Precompensation (In Nanoseconds)
500	125
300	208
250	250

7.3 ASYNCHRONOUS SERIAL COMMUNICATIONS CIRCUITS

The heart of the asynchronous serial communications circuit is a National Semiconductor NS16450 Asynchronous Communications Element (ACE). This device changes data received in a parallel format from the system to data in a serial format for a serial printer or other serial device. The NS16450 also performs the reverse function; changing data received in serial format to parallel format.

The NS16450 is I/O-mapped at ports 3F8h..3FFh or 2F8h..2FFh, depending on whether COM1 or COM2 is selected.

Placing jumper J1 in Position 1 selects Com1 and IRQ4. Placing jumper J1 in Position 2 selects Com2 and IRQ3.

The multipurpose controller jumpers are described in the section entitled "Jumpers." The I/O port addresses are given in Table 7-6.

Table 7-6. I/O Ports for Asynchronous Communications

Port 1	Port 2	Function
3F8h	2F8h	Receiver Buffer (when read by system), Transmitter Holding Register (when written to by system) OR
(See Note)		Baud Rate Divisor Latch
3F9h	2F9h	Interrupt Enable or
(See Note)		Baud Rate Divisor Latch
3FAh	2FAh	Interrupt ID (read only)
3FBh	2FBh	Line Control
3FCh	2FCh	Modem Control
3FDh	2FDh	Line Status
3FEh	2FEh	Modem Status
3FFh	2FFh	Reserved

Note: When bit 7 of the Line Control Register (LCR) is set (=1), writing to the first two ports programs the divisor rate for the Baud Rate Generator.

ACE RECEIVER BUFFER OR TRANSMITTER HOLDING REGISTER (3F8h)

This register contains the byte just received or the next byte to be transmitted by the ACE.

ACE BAUD RATE DIVISOR LATCH (3F8h, 3F9h)

The NS16450 contains a built-in baud rate generator that divides the input clock (1.8432 MHz) by a divisor to create a desired baud rate or serial transmission frequency.

The divisor is found according to the formula: Divisor = 1843200 / (Desired Baud Rate x 16).

Baud Rate	Divisor
110	1047
150	768
300	384
600	192
1200	96
2400	48
4800	24
9600	12

Setting Bit 7 (= 1) enables the first two I/O addresses of the Line Control Register as the addresses for the least- and most-significant bytes of the 16-bit baud rate divisor.

ACE INTERRUPT ENABLE REGISTER (3F9h)

The bits of this register enable up to four interrupt sources. The register format is:

BIT
76543210
1 = Received Data Available Interrupt enabled
1 = Transmitter Holding Register Empty Interrupt enabled
1 = Receiver Line Status Interrupt enabled
1 = Modem Status Interrupt enabled
0000 (Reserved)

ACE INTERRUPT ID REGISTER (3FAh, READ ONLY)

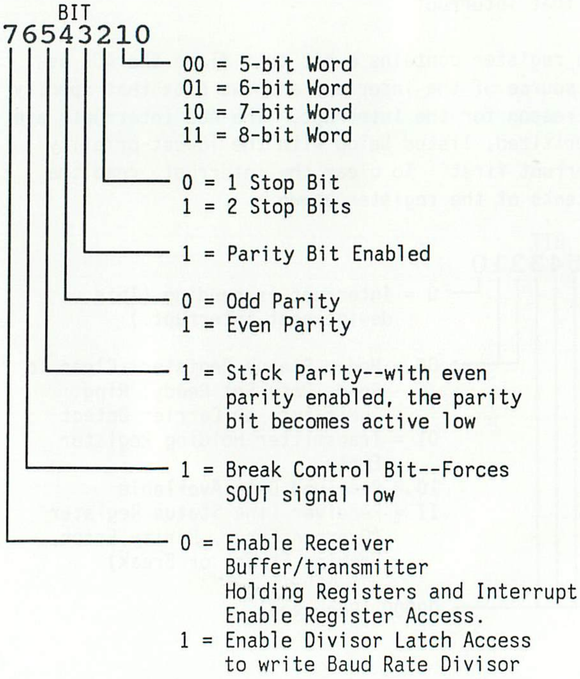
When a hardware interrupt occurs, the system searches for the device sending the interrupt and the reason for that interrupt.

This register contains a bit that flags the ACE as the source of the interrupt and two bits that specify the reason for the interrupt. The ACE interrupts are prioritized, listed below with the lowest-priority interrupt first. To clear the interrupt, read the contents of the register shown.

BIT
76543210
0 = Interrupt is pending (This device sent interrupt.)
00 = Modem Status Register--Clear To Send, Data Set Ready, Ring Indicator, or Carrier Detect
01 = Transmitter Holding Register Empty
10 = Received Data Available
11 = Receiver Line Status Register (Overrun Error, Parity Error, Framing Error, or Break)
00000 (Reserved)

ACE LINE CONTROL REGISTER (3FBh)

This register specifies the serial data transmission format.



BIT
76543210

00 = 5-bit Word
01 = 6-bit Word
10 = 7-bit Word
11 = 8-bit Word

0 = 1 Stop Bit
1 = 2 Stop Bits

1 = Parity Bit Enabled

0 = Odd Parity
1 = Even Parity

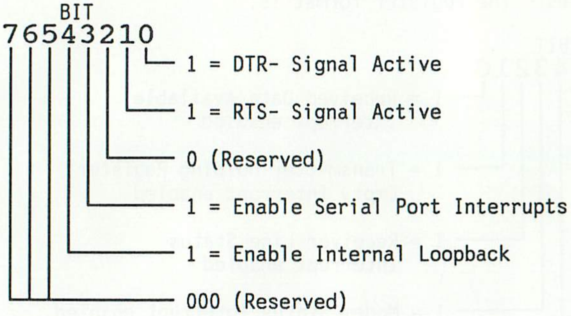
1 = Stick Parity--with even parity enabled, the parity bit becomes active low

1 = Break Control Bit--Forces SOUT signal low

0 = Enable Receiver Buffer/transmitter Holding Registers and Interrupt Enable Register Access.
1 = Enable Divisor Latch Access to write Baud Rate Divisor

ACE MODEM CONTROL REGISTER (3FCh)

This register controls the modem interface lines.



BIT
76543210

1 = DTR- Signal Active

1 = RTS- Signal Active

0 (Reserved)

1 = Enable Serial Port Interrupts

1 = Enable Internal Loopback

000 (Reserved)

ACE LINE STATUS REGISTER (3FDh, READ ONLY)

This register contains the status of the current data transfer.

BIT
76543210

1 = A character is in the Data register to be read

1 = Overrun Error--data lost

1 = Parity Error

1 = Framing Error

1 = When a Break Interrupt has occurred

1 = Transmitter Holding Register is empty, ready for character

1 = Transmitter Holding Register and Transmitter Shift Register are empty

0 (Reserved)

ACE MODEM STATUS REGISTER (3FEh, READ ONLY)

This register contains the status of the modem interface lines.

BIT
76543210

1 = CTS- has changed state since last read by the system

1 = DSR- has changed state since last read by the system

1 = RI- has changed state since last read by the system

1 = DCD- has changed state since last read by the system

1 = CTS- Signal Active

1 = DSR- Signal Active

1 = RI- Signal Active

1 = DCD- Signal Active

ACE RESERVED REGISTER (3FFh)

This register is not used currently.

7.4 PRINTER CIRCUITS

The printer port is enabled by setting Switch 2 in Switch Bank SW1 to the ON position. When the printer port is disabled, the printer port of a different controller can be used instead.

The printer circuits are addressed as ports. Data is sent in parallel to the printer, and printer status is received from the printer through these ports.

Before printing, the system must select the printer for output (through the Printer Control Register). For each byte sent to the printer:

1. The system checks the Printer Status Register. If the busy, paper out, or printer fault signals are active, the system either waits until the status changes or it shows an error message.
2. The system sends a byte of data to the Printer Data Register, then pulses the printer STROBE signal (through the Printer Control Register) for 500 ns (or more).
3. The system then monitors the Printer Status Register for acknowledgement of the data byte before sending the next byte.

In addition to data lines to the printer, the system also has several lines that control printer functions.

Printer functions are controlled by writing to or reading from I/O ports. The printer access I/O Ports are given in Table 7-7.

Table 7-7. I/O Ports For Printer Access

Port	R/W	Function
3BCh	R/W	Printer Data Register
3BDh	R	Printer Status Register
3BEh	R/W	Printer Control Register

PRINTER DATA REGISTER (3BCh)

Each byte written to the Printer Data Register (read or write) is latched into a loopback register and is sent to the printer. The register contents can be read back (for test purposes).

PRINTER STATUS REGISTER (3BDh, READ ONLY)

This register contains the current printer status.

BIT
76543210

000 (Reserved)
0 = Printer Error
1 = Printer Selected (on line)
1 = Out of Paper
0 = Printer acknowledges correct receipt of data byte
0 = Printer Busy

PRINTER CONTROL REGISTER (3BEh)

This register selects the printer for output, strobes the data into the printer, and performs other printer control functions.

BIT
76543210

1 = Printer Strobe
1 = Printer Auto Line Feed
0 = Initialize Printer
1 = Printer Select
1 = Enable Interrupt Bit
000 (Reserved)

7.5 JUMPERS

The Multipurpose Fixed Disk Controller jumpers are described in Table 7-8 and are shown in Figure 7-3.

Table 7-8. Multipurpose Fixed Disk Controller Jumpers

Jumper	Function
J1	Serial Port Base-Address and Interrupt Request Select. This address-selection option allows two serial ports to operate at the same time, using two I/O port ranges. Position 1, Com1-Serial Port 1 selected (3F8h and IRQ4 standard). Position 2, Com2-Serial Port 2 selected (2F8h and IRQ3).
J2	Diskette and Fixed Disk Drive Base-Address Select. This address selection option is available for special applications and under normal circumstances should not be changed. Position 1, Primary (Diskette1) Address Select (3F0h standard). Position 2, Secondary (Diskette2) Address Select (370h). "Diskette1 and Diskette2" are referencing the capabilities of using two addressable diskette controller boards, not diskette drives.

Note: To change the setting, remove the shunt jumper room the socket, rotate it 180 degrees, and reinstall the jumper in the socket.

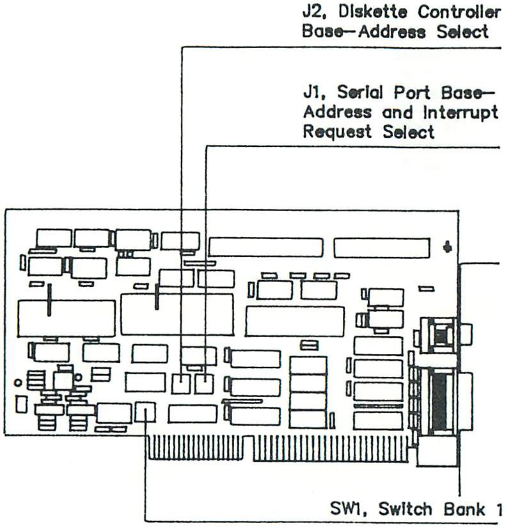

J2, Diskette Controller Base—Address Select
J1, Serial Port Base—Address and Interrupt Request Select
SW1, Switch Bank 1

Figure 7-3. Jumper Locations on Multipurpose Fixed Disk Controller

7.6 SWITCHES

The Multipurpose Fixed Disk Controller has one switch bank (SW1). These switches are described in Table 7-9.

Table 7-9. Controller Switches(SW1)

Number	Function
1	Fixed Disk Drive Enable. This switch allows the fixed disk drive port to be disabled. S1 = On, fixed disk drive port enabled (standard). S1 = Off, fixed disk drive port disabled.
2	Printer Enable. This switch allows the printer port to be disabled. This option prevents conflicts with I/O addresses 3BCh-3BFh when a multifunction board is installed that has a printer I/O port at these addresses. S2 = On, Parallel Printer Port enabled (standard). S2 = Off, Parallel Printer Port disabled.
3	Reserved Always Off.
4	Reserved Always Off.

7.7 CONNECTORS

The connector descriptions for the controller and the number of the table that contains the signal description for each connector are listed in Tables 7-10 through 7-15. The connector locations are shown in Figures 7-4 through 7-9. The Multipurpose Fixed Disk Controller signals used by the diskette drives are listed in Table 7-16.

Note: Pin 34 of the 34-conductor control cable is implemented as the DISKETTE CHANGE- signal. Diskette drives that use this pin for DRIVE READY- will not work.

Table 7-10. Multipurpose Controller Connectors

Connector	Description	Location of Signal Description
J701	Asynchronous Communication Connector	Table 7-11
J502	Parallel Printer Connector	Table 7-12
J902	Fixed Disk Drive LED	Table 7-13
J901	Fixed Disk Drive Controller Host Adapter Connector	Table 7-14
J501	Diskette Drive Connector	Table 7-15

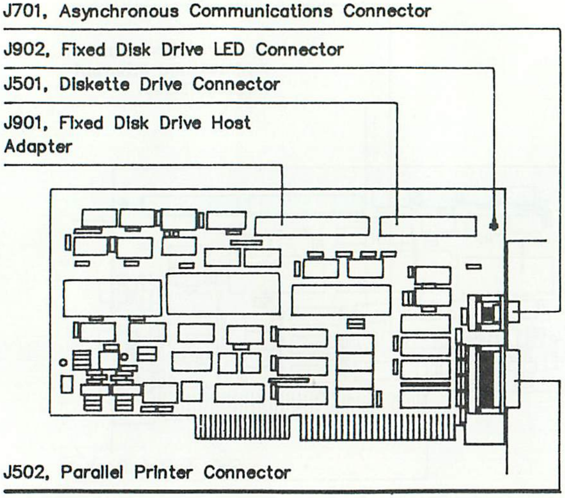

J701, Asynchronous Communications Connector
J902, Fixed Disk Drive LED Connector
J501, Diskette Drive Connector
J901, Fixed Disk Drive Host Adapter
J502, Parallel Printer Connector

Figure 7-4. Multipurpose Fixed Disk Controller Connectors

Table 7-11. J701, 9-Pin Serial Connector Signals

Signal	Pin	I/O	Description
CARRIER DETECT (CD)	1	I	Modem signal indicating that a connection is established with another modem
CLEAR TO SEND SEND (CTS)	8	I	Modem signal indicating readiness to accept data
DATA SET READY (DSR)	6	I	Modem signal--it is online and can receive data
DATA TERMINAL READY (DTR)	4	0	Signal to a modem indicating that the computer is ready
RECEIVE DATA (RX)	2	I	Serial data receive line
REQUEST TO SEND (RTS)	7	0	Signal to a modem to request a transmission
RING INDICATOR (RI)	9	I	Modem signal indicating that it is receiving a ringing signal from the phone line
SIGNAL GROUND	5	- -	- -
TRANSMIT DATA (TX)	3	0	Serial data sent to modem

Note: All signal levels are RS-232-C compatible.

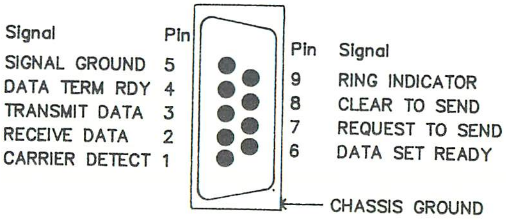


Figure 7-5. J701, 9-Pin Asynchronous Communications Connector

Table 7-12. J502, 25-Pin Parallel Printer Connector Signals

Signal	Pin	I/O	Description
ACKNOWLEDGE-	10	I	Data sent to printer has been received.
AUTO LINEFEED-	14	0	Instructs printer to automatically feed one line of paper after receiving a carriage return.
BUSY	11	I	Active-high signal indicating that the printer cannot receive data due to printing, offline, or error conditions.
DATA BIT 0	2	0	Signals transmit data to printer in 8-bit parallel format.
DATA BIT 1	3	0	
DATA BIT 2	4	0	
DATA BIT 3	5	0	
DATA BIT 4	6	0	
DATA BIT 5	7	0	
DATA BIT 6	8	0	
DATA BIT 7	9	0	
ERROR-	15	I	Indicates a printer error condition such as out-of-paper.
SIGNAL GROUND	18	-	Return conductors for all signals.
	19	-	
	20	-	
	21	-	
	22	-	
	23	-	
	24	-	
	25	-	

(Continued)

Table 7-12. J502, 25-Pin Parallel Printer Connector Signals (Concluded)

Signal	Pin	I/O	Description
INITIALIZE PRINTER-	16	0	Initializes the printer and clears the print buffer. This signal should remain active for at least 500 us.
PAPER END	12	I	Indicates that the printer is out of paper.
SELECT	13	I	Indicates that the printer is selected and online.
SELECT IN-	17	0	Selects the printer and enables it to accept data.
STROBE-	1	0	On high-to-low transition, causes data present on DATA BIT lines to be loaded into printer. STROBE- pulse width must be a minimum of 500 ns. Data must be setup a minimum of 500 ns before the high-to low transition and held a minimum of 500 ns after the low-to-high transition.

Note: All signals are TTL-level.

Table 7-13. J902, Fixed Disk Drive Controller LED Indicators

Signal	Pin	I/O	Description
LEDANODE	1		+5 VDC source for the fixed disk drive LED indicator.
- -	2		Reserved
ACTIVE-	3	0	Indicates that the fixed disk drive is being accessed. This line is used to drive an activity LED indicator that lights when the drive is activated.
- -	4		Reserved

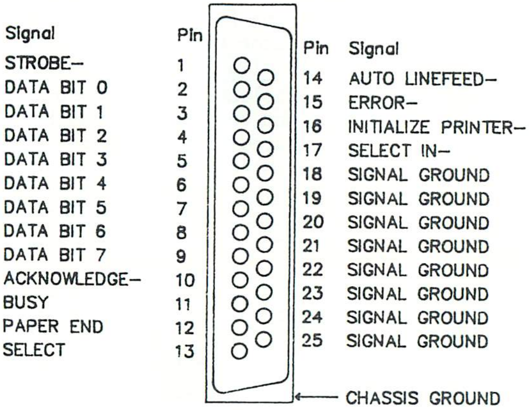


Figure 7-6. J502, 25-Pin Parallel Printer Connector

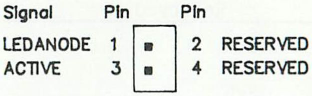


Figure 7-7. J902, Fixed Disk Drive Controller LED Indicators Connector

Table 7-14. J901, Fixed Disk Drive Controller Host Adapter Connector Signal Descriptions

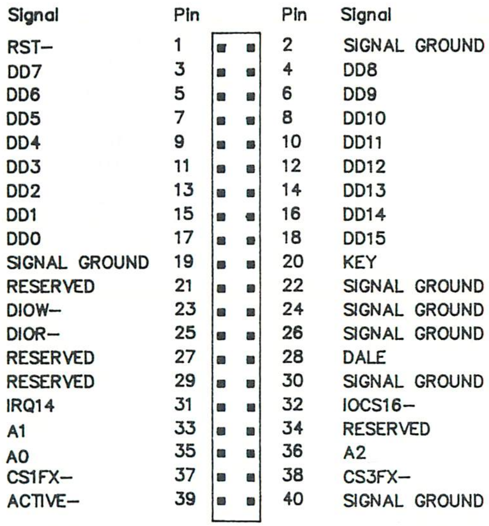
Signal	Pin	I/O	Description
ACTIVE-	39	I	Active-low signal indicating that the fixed disk drive LED indicator is on and the fixed disk drive is being accessed.
CS1FX-	37	0	Chip Select 1Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 1F0h and 1F7h.
CS3FX-	38	0	Chip Select 3Fx. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 3F6h through 3F7h.
DA0	35	0	Address A0-A2. Buffered address lines from the address bus to the fixed disk drive controller.
DA1	33		
DA2	36		
DALE	28	0	Address latch enable. Signals that address bus signals are stable and valid.
DD7	3	0	Data bit 0-7. Least-significant eight bits of the 16-bit data bus for data and status communication between the controller and the host. D7 is the most-significant bit of this byte.
DD6	5	0	
DD5	7	0	
DD4	9	0	
DD3	11	0	
DD2	13	0	
DD1	15	0	
DD0	17	0	

(Continued)

Table 7-14. J901, Fixed Disk Drive Controller Host Adapter Connector Signal Descriptions (Concluded)

Signal	Pin	I/O	Description
DD8	4	O	Data bit 8-15. Most-significant eight bits for data and status communication between the controller and the host. DD15 is the most-significant bit of this byte.
DD9	6	O	
DD10	8	O	
DD11	10	O	
DD12	12	O	
DD13	14	O	
DD14	16	O	
DD15	18	O	
DIOW-	23	O	I/O write. Active when the host writes a control byte or data word to the controller.
DIOR-	25	I	I/O read. Active when the host reads a status byte or data word from the controller.
I/016CS-	32	O	Chip Select 16. Chip select used to signal the processor that the current I/O cycle is a 16-bit, single wait-state cycle.
IRQ14	31	I	Interrupt Request 14. Asserted by the controller to interrupt the processor upon completion of a fixed disk operation.
RST-	1	O	Reset. This signal resets the controller to the initial power-on condition.
SIGNAL GROUND	2,19, 22,24, 26,30,40	-	Return conductor.

Note: Pins 20, 21, 27, 29, and 34 are not connected.



Signal	Pin	Pin	Signal
RST–	1	2	SIGNAL GROUND
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
SIGNAL GROUND	19	20	KEY
RESERVED	21	22	SIGNAL GROUND
DIOW–	23	24	SIGNAL GROUND
DIOR–	25	26	SIGNAL GROUND
RESERVED	27	28	DALE
RESERVED	29	30	SIGNAL GROUND
IRQ14	31	32	IOCS16–
A1	33	34	RESERVED
A0	35	36	A2
CS1FX–	37	38	CS3FX–
ACTIVE–	39	40	SIGNAL GROUND

Figure 7-8. J901, Fixed Disk Drive Controller Host Adapter Connector

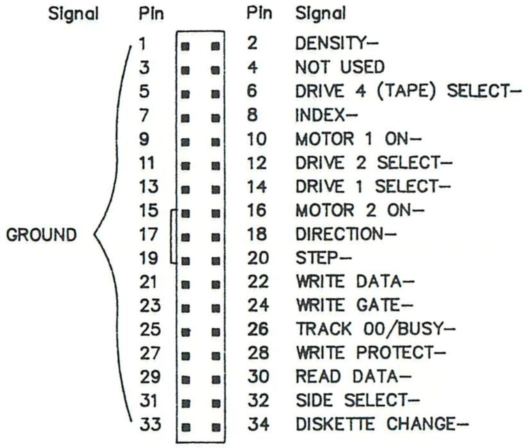
Table 7-15. J501, Diskette Drive Controller Signal Connector Descriptions

Signal	Pin	I/O	Description
DENSITY-	2	O	Not used on a 360-KB diskette drive.
DIRECTION-	18	O	Selects the direction to step the head when a step pulse is issued.
DISKETTE CHANGE-	34	I	Indicates that the drive door has been opened.
DRIVE 1 SELECT- DRIVE 2 SELECT- DRIVE 4(TAPE)SELECT-	14 12 6	O O O	Allows the selection of a drive so that it can respond to the interface signals.
INDEX-	8	I	(Diskette) Indicates to the drive controller that the media index opening is under the index sensor.
MOTOR1 ON-	10	O	Activates the drive motor.
MOTOR2 ON-	16	O	Activates the drive motor.

(Continued)

Table 7-15. J501, Diskette Drive Controller Signal Connector Descriptions (Concluded)

Signal	Pin	I/O	Description
READ DATA-	30	I	This is the data-stream read from the drives and contains clock and data signals.
SIDE SELECT-	32	O	Selects Side 0 (Head 0) or Side 1 (Head 1).
STEP-	20	O	(Diskette) Tells the drive to step the heads one track.
TRACK 00-/BUSY-	26	I	(Diskette) Indicate-to the controller that the heads are at Track 0.
WRITE DATA-	22	O	This stream of data is written to the drive when WRITE GATE- signal is enabled.
WRITE GATE-	24	O	Enables the drive's write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	28	I	Indicates to the drive controller that the media is write protected.



Signal	Pin	Pin	Signal
GROUND	1	2	DENSITY–
	3	4	NOT USED
	5	6	DRIVE 4 (TAPE) SELECT–
	7	8	INDEX–
	9	10	MOTOR 1 ON–
	11	12	DRIVE 2 SELECT–
	13	14	DRIVE 1 SELECT–
	15	16	MOTOR 2 ON–
	17	18	DIRECTION–
	19	20	STEP–
	21	22	WRITE DATA–
	23	24	WRITE GATE–
	25	26	TRACK 00/BUSY–
	27	28	WRITE PROTECT–
	29	30	READ DATA–
	31	32	SIDE SELECT–
	33	34	DISKETTE CHANGE–

Figure 7-9. J501, Diskette Drive Controller Connector

Table 7-16. Multipurpose Controller Signals Used by the Diskette Drives

Controller		Diskette Drive 1		Diskette Drive 2		40-MB Fixed Disk Drive Back-up	
Pin	Function	Pin	Function (Note 1)	Pin	Function	Pin	Function
2	DENSITY-	2	DENSITY- (Note 2)	2	DENSITY-	2	DENSITY-
4	Not used	4	Not used	4	Not used	4	Not used
6	DRIVE 4 (TAPE) SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-	6	DRIVE 4 SELECT-
8	INDEX-	8	INDEX-	8	INDEX-	8	INDEX-
10	MOTOR 1 (A) ON-	10	MOTOR 2 ON-(Note 3)	10	MOTOR 1 ON-	10	MOTOR 2 ON-
12	DRIVE 2 (B) SELECT-	12	DRIVE 1 SELECT-(Note 3)	12	DRIVE 2 SELECT-	12	DRIVE 1 SELECT-
14	DRIVE 1 (A) SELECT-	14	DRIVE 2 SELECT-(Note 3)	14	DRIVE 1 SELECT-	14	DRIVE 2 SELECT-
16	MOTOR 2 (B) ON-	16	MOTOR 1 ON-(Note 3)	16	MOTOR 2 ON-	16	MOTOR 1 ON-
18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-	18	DIRECTION SELECT-
20	STEP-	20	STEP-	20	STEP-	20	STEP-
22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-	22	WRITE DATA-
24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-	24	WRITE GATE-
26	TRACK 00-/BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-	26	TRACK 00-/ BUSY-
28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-	28	WRITE PROTECT-
30	READ DATA-	30	READ DATA-	30	READ DATA-	30	READ DATA-
32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-	32	SIDE SELECT-
34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-	34	DISKETTE CHANGE-

Notes:
1. The order of the columns does not reflect the order of the connectors on the diskette disk drive cable.
2. Shaded areas denote functions unused on that drive.
3. The diskette drive cable interchanges pin 10 with pin 16 and pin 12 with pin 14 for Diskette Drive 1.

7.8 SCHEMATICS

The schematics for the Multipurpose Fixed Disk Controller are shown in Figure 7-10. COMPAQ Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the operation of the controller.

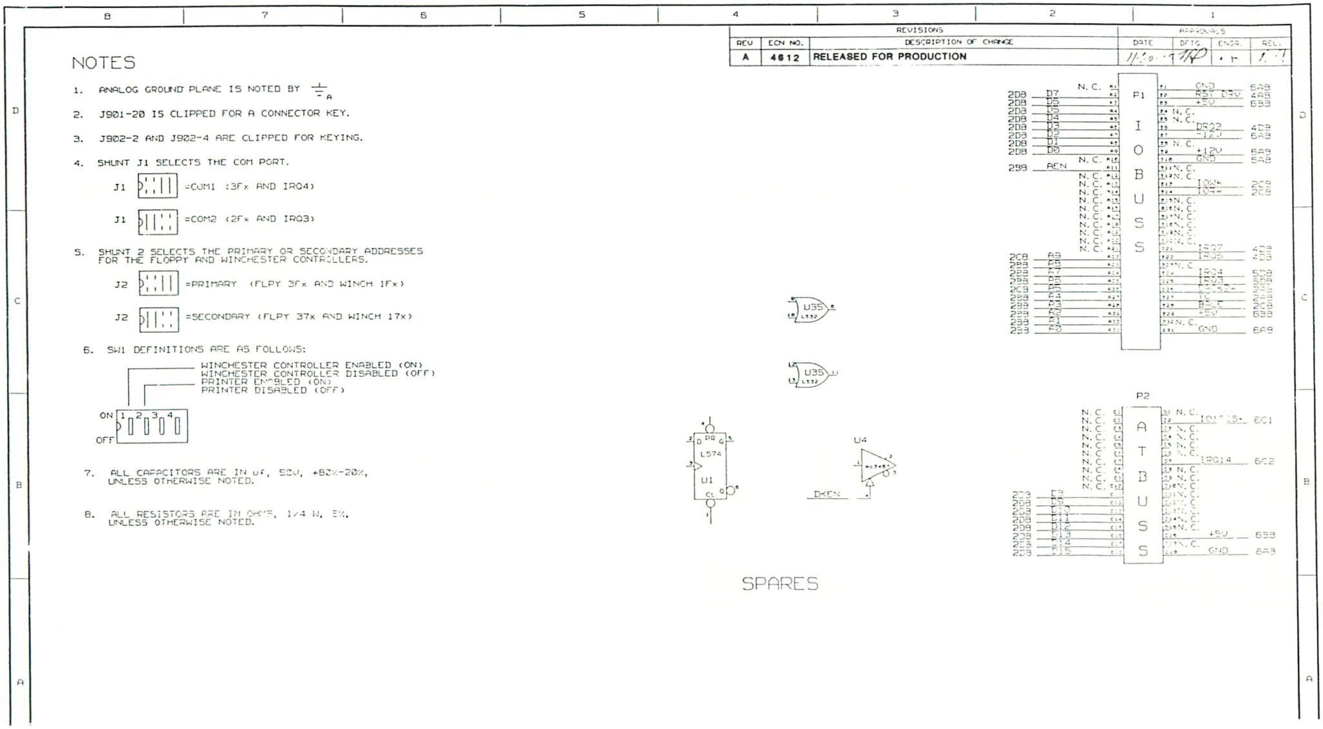

8
7
6
5
4
3
2
1
D
C
B
A
REVISIONS
REV
ECN NO.
DESCRIPTION OF CHANGE
A
4612
RELEASED FOR PRODUCTION
APPROVALS
DATE
DFTG.
ENGR.
REL.
NOTES
1. ANALOG GROUND PLANE IS NOTED BY
2. J901-20 IS CLIPPED FOR A CONNECTOR KEY.
3. J902-2 AND J902-4 ARE CLIPPED FOR KEYING.
4. SHUNT J1 SELECTS THE COM PORT.
J1 =COM1 (3Fx AND IRQ4)
J1 =COM2 (2Fx AND IRQ3)
5. SHUNT 2 SELECTS THE PRIMARY OR SECONDARY ADDRESSES FOR THE FLOPPY AND WINCHESTER CONTROLLERS.
J2 =PRIMARY (FLPY 3Fx AND WINCH 1Fx)
J2 =SECONDARY (FLPY 37x AND WINCH 17x)
6. SW1 DEFINITIONS ARE AS FOLLOWS:
WINCHESTER CONTROLLER ENABLED (ON)
WINCHESTER CONTROLLER DISABLED (OFF)
PRINTER ENABLED (ON)
PRINTER DISABLED (OFF)
ON 1 2 3 4
OFF
7. ALL CAPACITORS ARE IN uF, 50V, +80%-20%, UNLESS OTHERWISE NOTED.
8. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%, UNLESS OTHERWISE NOTED.
P1
I O B U S S
D7
D6
D5
D4
D3
D2
D1
D0
AEN
N. C.
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
2D8
2B8
2C8
GND
RST DRV
+5V
-5V
DRQ2
-12V
+12V
IOW*
IOR*
IRQ7
IRQ5
IRQ4
IRQ3
BALE
6A8
4A8
6B8
4D8
5A8
2C8
4D8
5D8
U35
LS32
U1
LS74
PR
CL
U4
DKEN
P2
A T B U S S
IO16
IRQ14
6C1
6C2
6B8
6A8
SPARES

Figure 7-10. Multipurpose Fixed Disk Controller Schematics (Page 1 of 6)

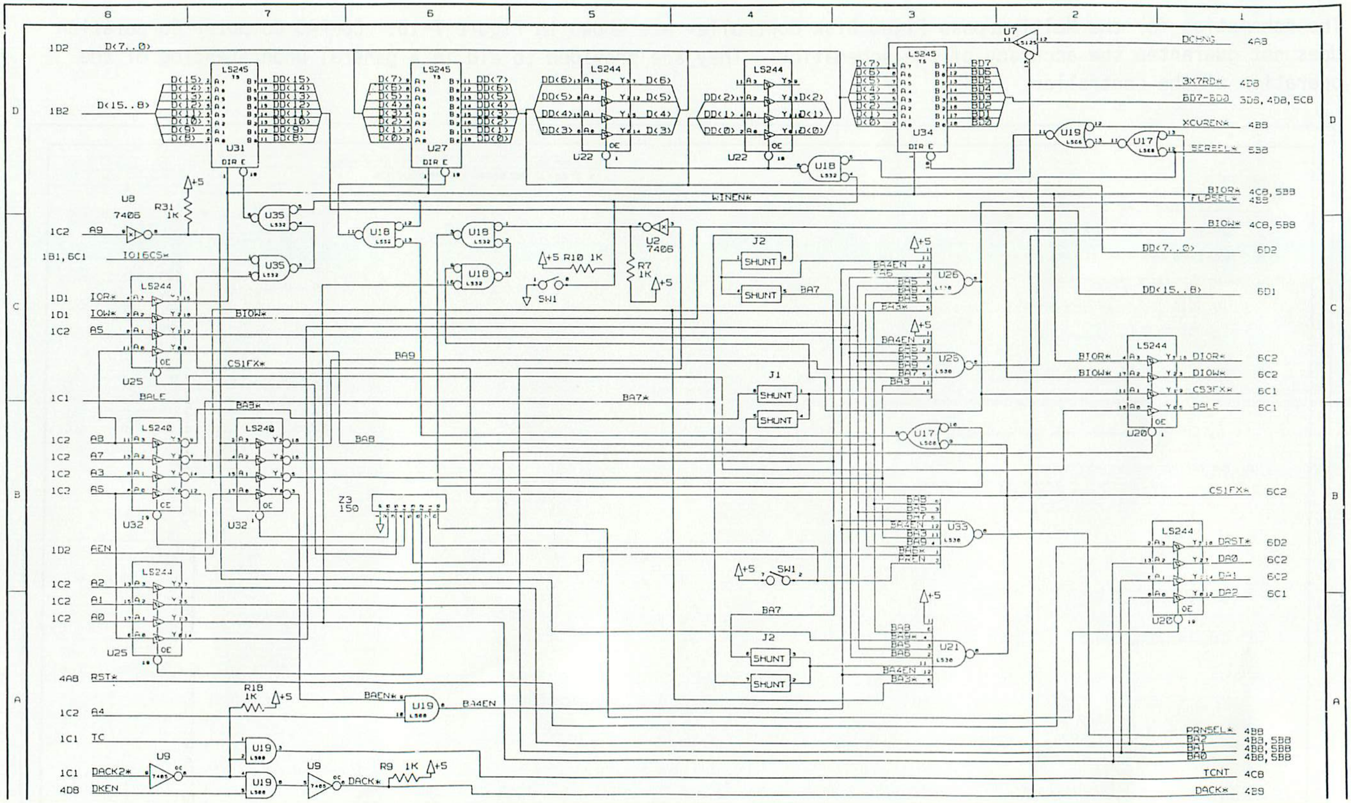


Figure 7-10. Multipurpose Controller Schematics (Page 2 of 6)

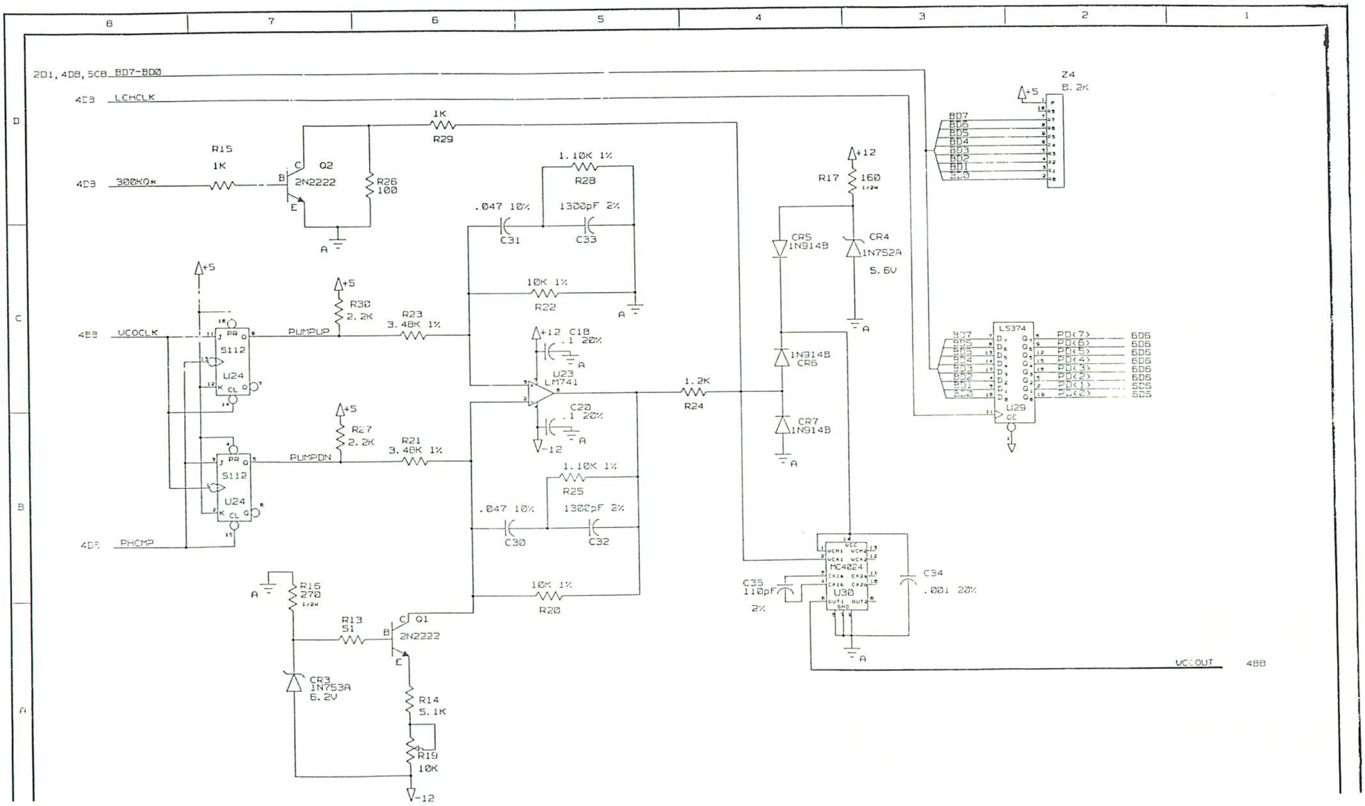


Figure 7-10. Multipurpose Controller Schematics (Page 3 of 6)

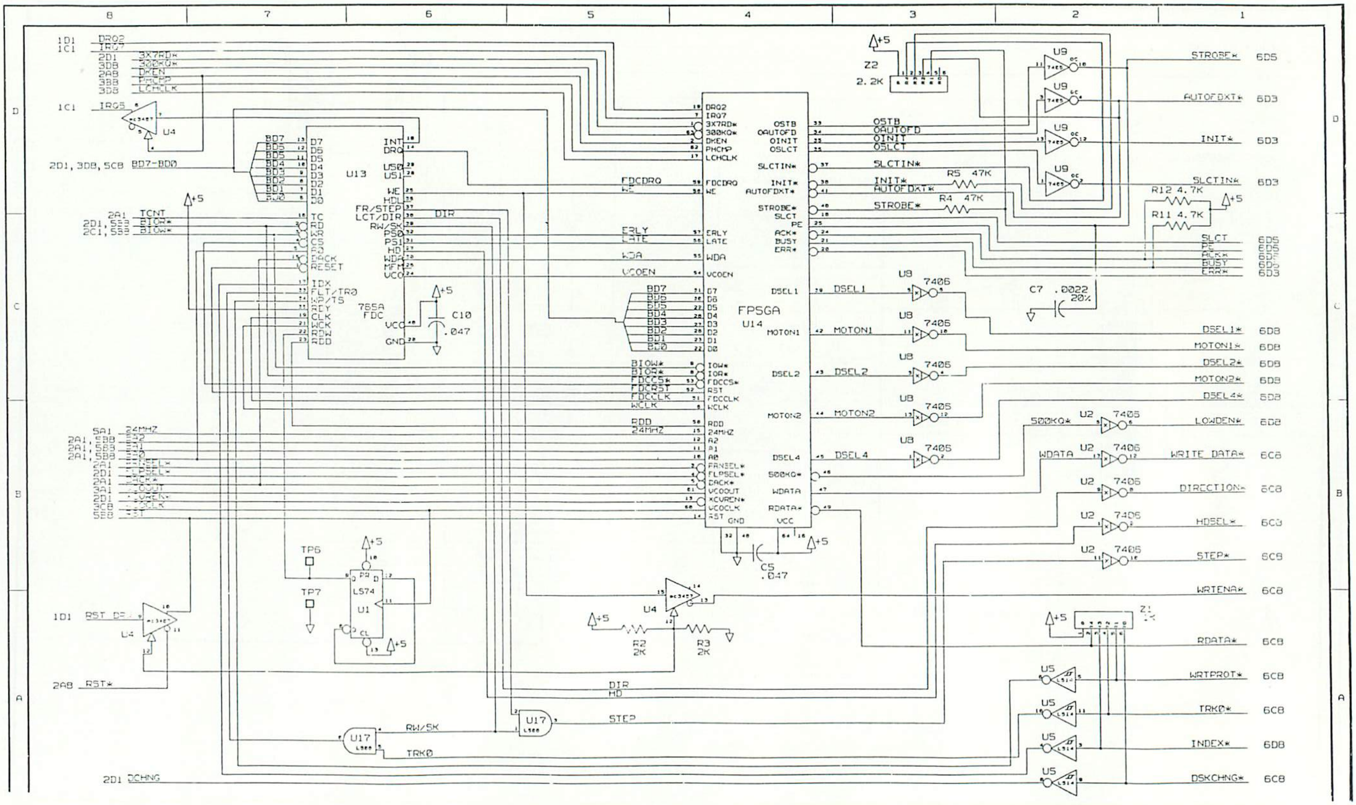


Figure 7-10. Multipurpose Controller Schematics (Page 4 of 6)
]

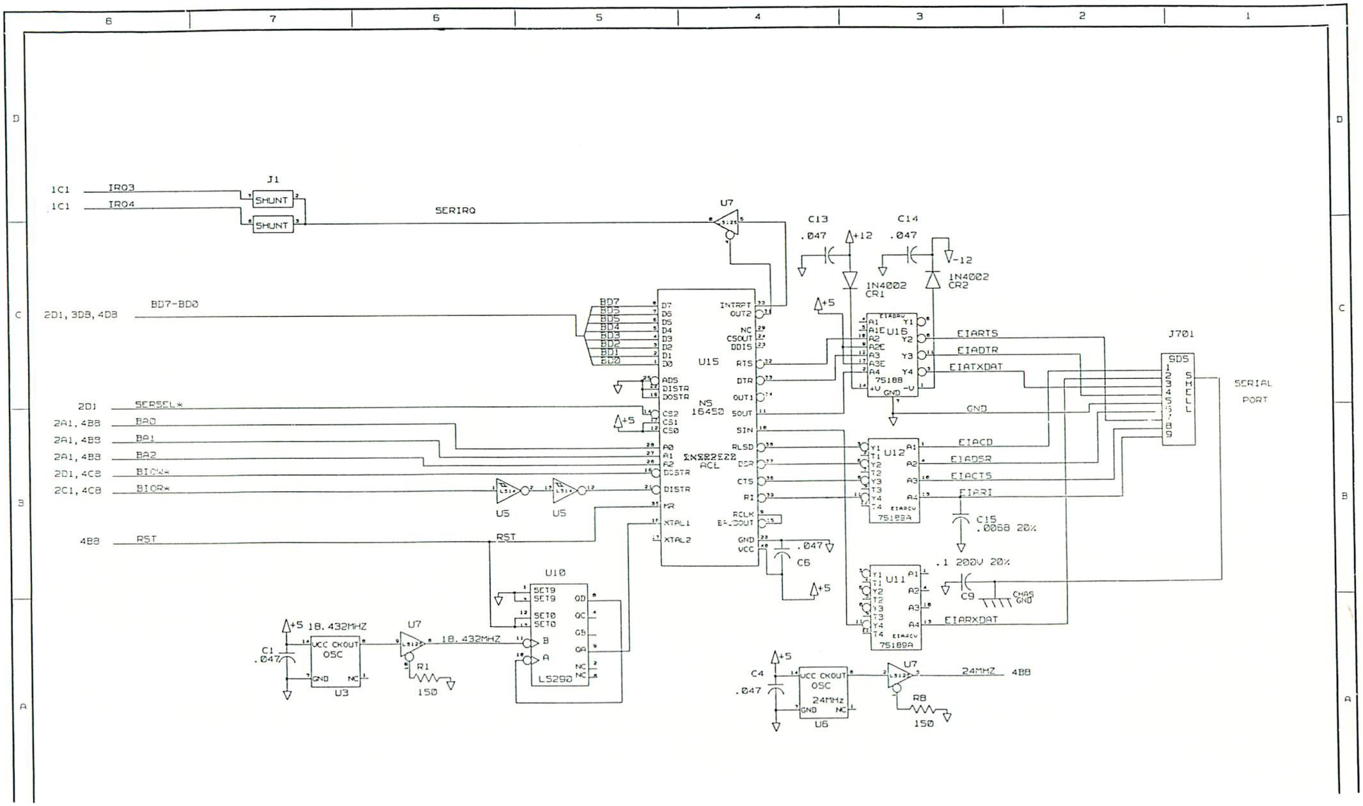


Figure 7-10. Multipurpose Controller Schematics (Page 5 of 6)

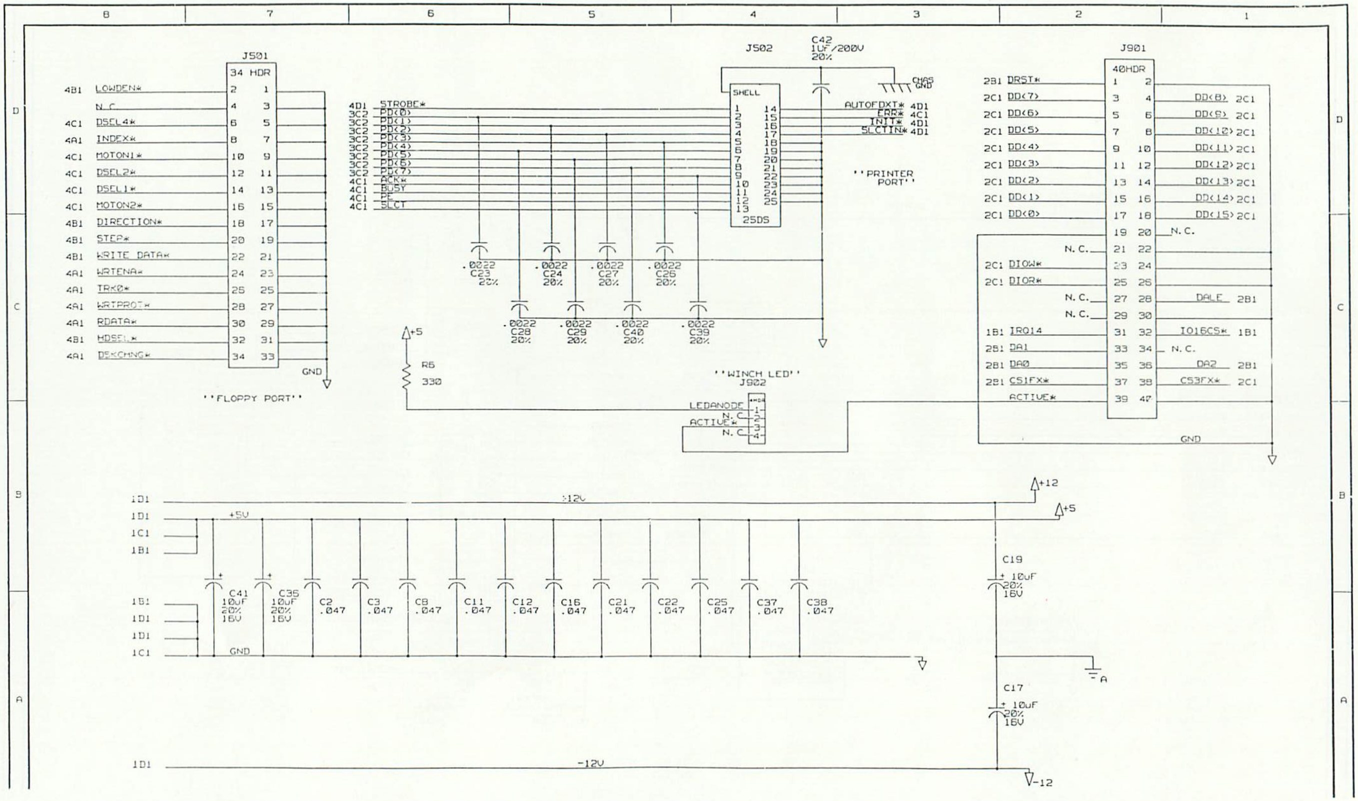


Figure 7-10. Multipurpose Controller Schematics (Page 6 of 6)

Chapter 8
DISKETTE DRIVES

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Chapter 8
DISKETTE DRIVES

8.1 INTRODUCTION

The COMPAQ DESKPRO 386 provides a 5.25-inch (in.) diskette drive capable of storing 1.2 MB of data per diskette. COMPAQ DESKPRO 386 offers an optional second diskette drive that stores either 360 KB or 1.2 MB of data per diskette.

The diskette drive main chassis contains the:

- Diskette drive motor
- Stepper motor
- Head-carriage assembly
- Spindle
- Diskette drive logic board
- Left and right diskette guides
- Front bezel
- Front-door mechanism

Figure 8-1 shows a typical diskette drive chassis.

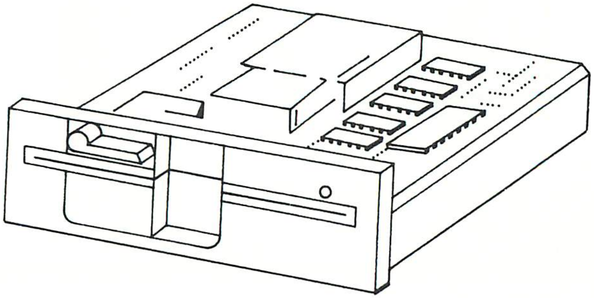


Figure 8-1. Typical Diskette Drive Chassis

The diskette drive logic board controls the diskette drive motor speed, read and write circuits, and other electronic circuits.

Figure 8-2 is a functional block diagram for a diskette drive.

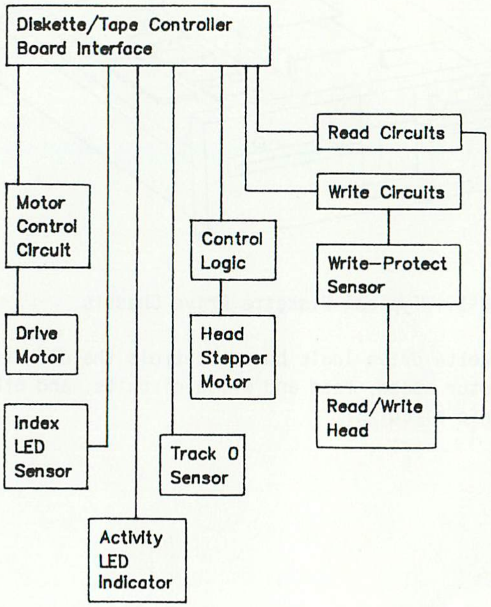


Figure 8-2. Diskette Drive Functional Block Diagram

Multiple diskette drives connect in a daisy-chain manner (one after another on the same cable) to the multipurpose fixed disk controller board.

The position (or location) of the drive on the controller cable determines diskette drive A or B selection. Both diskette drives configured as the second physical diskette drive must have jumper DS1 (drive select 1) installed. Jumpers DS0, DS2, and DS3 are not installed.

For systems with a 360-KB diskette drive and a 1.2-MB diskette drive, the terminating resistor should always be on the 1.2-MB diskette drive.

For systems with two 1.2-MB diskette drives, diskette drive A should contain the terminating resistors (resistor pack). There should be no resistor pack in diskette drive B.

8.2 FUNCTIONAL DESCRIPTION

1.2-MB Diskette Drive

The 1.2-MB diskette drive is a high-capacity diskette drive with the following features:

- Half-height, 5.25-in. diskette drive
- Two transfer rates--300 kb/s (double density) or 500 kb/s (high density)
- Data storage on 80 tracks (96 TPI)

To read or write to 48-TPI media, the software must step the 96-TPI drive head twice between each 48-TPI track. Because the track width of the 96-TPI diskette drive is approximately half the track width of the 48-TPI diskette drive, standard 48-TPI diskette drives may not be able to read diskettes written by the 96-TPI drive in the 48-TPI format.

360-KB Diskette Drive

The 360-KB diskette drive has the following features:

- Half-height, 5.25-in. diskette drive
- Double-sided, double-density (DSDD) 40 tracks (48-TPI)

The location of the drive on the controller cable determines diskette drive A or B selection. Both diskette drives are configured as the second physical diskette drive. Drive-select 2 (jumper) should be installed on both diskette drives. Drive-select 1, 3, and 4 (jumpers) are not installed.

Some models of diskette drives refer to drive-select jumpers as DS0, DS1, DS2, and DS3, in which case, DS1 should be selected.

Diskette drive A should always contain the terminating resistors (resistor pack). There should be no resistor pack in diskette drive B.

8.3 SPECIFICATIONS

Table 8-1 lists the physical and electrical specifications for both the 1.2-MB and 360-KB diskette drives.

Table 8-1. Diskette Drive Physical and Electrical Specifications

	1.2-MB Diskette Drive	360-KB Diskette Drive
Size:		
Width	5.8 in. (146 mm)	5.8 in. (146 mm)
Height	1.6 in. (41 mm)	1.6 in. (41 mm)
Depth	8 in. (203 mm)	8 in. (203 mm)
Capacity:		
Unformatted	1,600,000 bytes	500,000 bytes
Formatted	1,228,800 bytes	368,640 bytes
Flux reversal density	9875 FR/I (Track 79)	5876 FR/I (Track 39)
Data-transfer rate	500 kb/s	250 kb/s
Sectors/track	15	9
Bytes/sector	512	512
Seek time:		
Track-to-track	3 ms	6 ms
Average	79 ms	80 ms
Settling time	15 ms	15 ms
Rotational Speed	360 RPM ±1.0%	300 RPM ±1.5%
Motor Start Time	500 ms	500 ms

8.4 CONNECTORS

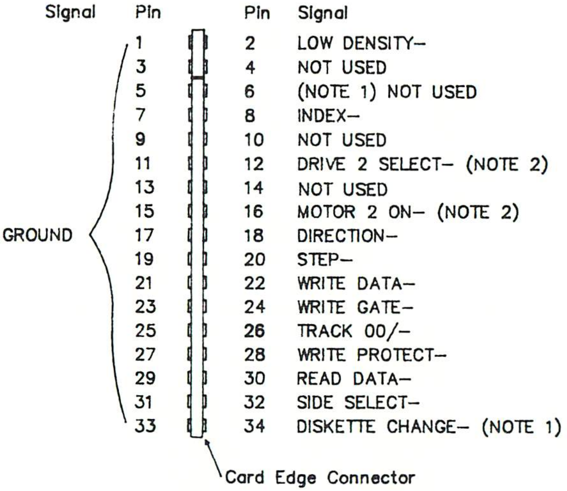
Table 8-2 lists the diskette drive control signals.

Table 8-2. Diskette Drive Control Signals

Signal	Pin	I/O	Description
LOW DENSITY-	2	I	When using high-capacity (1.2-MB) drives, this signal selects High (500 kb/s) or Low (300 kb/s) mode (see Note).
DIRECTION-	18	I	Selects the direction in which to move the head when a step pulse is issued.
DISKETTE CHANGE-	34	0	Indicates to diskette drive controller that the drive door has been opened (and possibly different media installed). (See Note.)
DRIVE 2 SELECT-	10	I	Allows the selection of a diskette drive so that it can respond to the interface signals.
INDEX-	8	0	Indicates to the diskette drive controller that the media index hole is under the index sensor.
MOTOR 2 ON-	16	I	Activates the drive motor.
READ DATA-	30	0	This is the data-stream read from the diskette containing clock and data signals.
SIDE SELECT-	32	I	Selects side 0 (Head 0) or side 1 (Head 1).
STEP-	20	I	Tells the diskette drive to step the heads one track.
TRACK 00-	26	0	Indicates to the diskette drive controller that the heads are at Track 0.
WRITE DATA-	22	I	This stream of data is written to the diskette when WRITE GATE- is enabled.
WRITE GATE-	24	I	Enables the diskette drive write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	28	0	Indicates to the diskette drive controller that the media is write-protected.

Note: The DENSITY- and DISKETTE CHANGE- signals are not used on 360-KB (48-TPI) diskette drives.

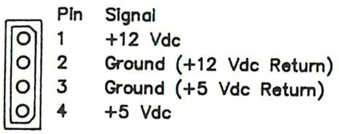
Figures 8-3 and 8-4 show the pinouts of the diskette drive connectors.



Signal	Pin	Pin	Signal
GROUND	1	2	LOW DENSITY–
	3	4	NOT USED
	5	6	(NOTE 1) NOT USED
	7	8	INDEX–
	9	10	NOT USED
	11	12	DRIVE 2 SELECT– (NOTE 2)
	13	14	NOT USED
	15	16	MOTOR 2 ON– (NOTE 2)
	17	18	DIRECTION–
	19	20	STEP–
	21	22	WRITE DATA–
	23	24	WRITE GATE–
	25	26	TRACK 00/–
	27	28	WRITE PROTECT–
	29	30	READ DATA–
	31	32	SIDE SELECT–
	33	34	DISKETTE CHANGE– (NOTE 1)

Notes:
1. Not applicable on 360-KB diskette drives.
2. DRIVE 2 SELECT– and MOTOR 2 ON– are the signals supplied by the diskette/tape controller for Diskette Drive 2 (B). If the diskette drive is Diskette Drive 1(A), the signals from the diskette/tape controller will be DRIVE 1 SELECT– and MOTOR 1 ON–

Figure 8-3. Diskette Drive Control Connector Pinout



Pin	Signal
1	+12 Vdc
2	Ground (+12 Vdc Return)
3	Ground (+5 Vdc Return)
4	+5 Vdc

Figure 8-4. Diskette Drive Power Connector Pinout

Chapter 9

FIXED DISK DRIVE SYSTEMS

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Chapter 9
FIXED DISK DRIVE SYSTEMS

9.1 INTRODUCTION

The fixed disk drive systems provide mass data storage for the COMPAQ DESKPRO 386.

Fixed disk drives:

- Are sealed units. The media (disk surfaces) are not removable.
- Rotate the media at 3600 RPM
- Have a much higher data-transfer rate and faster access time than diskette drives.

A fixed disk drive has two major components:

- A sealed head-disk assembly containing the disk platters, heads, and drive motor
- A drive-logic circuit board that controls the fixed disk drive's motors and the read and write electronics.

A fixed disk drive system includes a fixed disk drive and a fixed disk drive controller. Some fixed disk drive systems incorporate the controller circuitry onto the logic board of the fixed disk drive.

A fixed disk drive controller is I/O mapped into specific I/O addresses. Generally, a jumper on the fixed disk drive controller specifies the base I/O address for that controller.

The fixed disk drive controller responds to commands given to it, and takes control of the system as needed to transfer information.

Two fixed disk drive controllers cannot occupy the same I/O addresses without causing bus contention and possibly damaging the system.

Fixed Disk Drive Types

Fixed disk drives vary in the number of heads, cylinders, platters, and so on. Each fixed disk drive has a list of parameters that the computer must know to control the fixed disk drive. These parameters are stored in ROM on the system board.

The SETUP program is used to specify which type of fixed disk drive is installed in the system. SETUP stores the fixed disk drive type in the CMOS configuration memory on the system board. SETUP can be found on the USER PROGRAMS diskette.

The COMPAQ DESKPRO 386 supports two types of fixed disk drive types. The parameters for these drives have been optimized to complement the high performance of the other COMPAQ DESKPRO 386 subsystems. The 40-MB and 130-MB fixed disk drives have the speed and capacity required by the power applications for which the COMPAQ DESKPRO 386 is best suited.

The 40-MB fixed disk drive provides a 5 mb/s data-transfer rate with an average access time of less than 30 ms. This average access time over the 40-MB data capacity makes this drive perform exceptionally well in disk-intensive applications that perform non-sequential disk accesses. Data bases are typical of the applications in this category.

The 130-MB fixed disk drive provides unequaled performance and capacity in personal computer class products. This drive provides a 10 mb/s data transfer rate with an average access time of less than 25 ms over the 130-MB drive capacity. This drive is particularly well-suited for applications such as file servers that require maximum performance and capacity in disk storage.

The 40-MB fixed disk drive is a type 17, and the 130-MB fixed disk drive is a type 25.

Table 9-1 lists the typical values for the fixed disk drive parameter table including the drive types and formatted capacities. The values (such as number of heads and cylinders) for the other drive types are subject to change.

Table 9-1. Fixed Disk Drive Types

Drive Type	Cyl-inders	Max Heads	Pre-Comp Cyl.	Landing Zone Cyl.	Sectors/ Track	Cap-pacity (MB)
1	306	4	128	305	17	10.65
2	615	4	128	638	17	21.41
3	615	6	128	615	17	32.12
4	1024	8	512	1023	17	71.30
5	940	6	512	939	17	49.09
6	697	5	128	696	17	30.33
7	462	8	256	511	17	32.17
8	925	5	128	924	17	40.26
9	900	15	-1	899	17	117.50
10	980	5	-1	980	17	42.65
11	823	10	-1	822	17	71.63
12	925	9	128	924	17	72.46
13	612	8	256	611	17	42.61
14	754	11	-1	753	17	72.19
15	0	0	0	0	0	0
16	612	4	0	612	17	21.31
17	980	5	128	980	17	42.65
18	966	6	128	966	17	50.45
19	1023	8	-1	1023	17	71.23
20	733	5	256	732	17	31.90
21	733	7	256	732	17	44.66
22	768	6	-1	768	17	40.11
23	771	6	-1	771	17	20.16
24	966	14	-1	966	17	117.71

Note: A value of -1 for the Write Precompensation Cylinder byte means that no write precompensation is used.

(Continued)

Table 9-1. Fixed Disk Drive Types (Concluded)

Drive Type	Cyl-inders	Max Heads	Pre-Comp Cyl.	Landing Zone Cyl.	Sectors/ Track	Cap-pacity (MB)
25	966	16	-1	966	17	134.53
26	1023	14	-1	1023	17	124.66
27	966	10	-1	966	17	84.08
28	771	3	-1	771	17	20.11
29	578	4	-1	578	17	20.09
30	615	4	128	615	25	31.49
31	615	8	128	615	25	62.98
32	966	3	-1	966	34	50.45
33	966	5	-1	966	34	84.08
34	966	7	-1	966	34	117.71
35	966	8	-1	966	34	134.53
36	966	9	-1	966	34	151.35
37	966	5	-1	966	34	84.08
38	1023	9	-1	1023	33	155.56
39	1023	11	-1	1023	33	190.13
40	1023	13	-1	1023	33	224.70
41	1023	15	-1	1023	33	259.27
42	1023	16	-1	1023	34	284.93
43	756	4	-1	756	26	40.26
44	756	2	-1	756	26	20.13
45	756	4	-1	768	26	40.89
46	768	2	-1	768	26	20.45
47	966	5	128	966	25	61.82

Note: A value of -1 for the Write Precompensation Cylinder byte means that no write precompensation is used.

Configurations

The 40- and 130-MB fixed disk drive systems for the COMPAQ COMPAQ DESKPRO 386 are mutually exclusive. One system or the other can be used, but not both. This is because 1) the 130-MB fixed disk drive system uses an Enhanced Small Device Interface (ESDI) fixed disk drive controller and an ESDI-compatible fixed disk drive, and 2) a system cannot have two fixed disk drive controllers mapped into the same I/O addresses.

The COMPAQ DESKPRO 386 can have three different fixed disk drive configurations:

- One 40-MB fixed disk drive system
- Two 40-MB fixed disk drive systems
- One 130-MB fixed disk drive system

Fixed Disk Drive Programming

All fixed disk drive systems are fully-compatible, which means that the I/O addresses, registers, and command structures are all the same.

This section presents information that is the same for all fixed disk drive systems. The information that changes with each type of fixed disk drive or fixed disk drive system is presented later in this chapter.

Registers

Table 9-2 lists the standard and alternate I/O addresses for a fixed disk drive controller.

Table 9-2. Fixed Disk Drive Controller I/O Addresses

I/O Address 1	2	R/W	Register
1F0h	170h	R/W	Data
1F1h	171h	R	Error
1F1h	171h	W	Write Precompensation
1F2h	172h	R/W	Sector Count
1F3h	173h	R/W	Sector Number
1F4h	174h	R/W	Cylinder LOW
1F5h	175h	R/W	Cylinder HIGH
1F6h	176h	R/W	Sector Size/Drive Select/Head
1F7h	177h	R	Status
1F7h	177h	W	Command
3F6h	376h	R	Alternate Status
3F6h	376h	W	Drive Control
3F7h	377h	R	Drive Address (see Note)
3F7h	377h	W	Not decoded or used

Note: Only bits D<6..0> are resident on the fixed disk drive controller. Bit 7 of this I/O address is resident on the diskette/tape controller.

DATA (1F0h)

All data to the fixed disk drive controller passes through the Data register. It is also the port to which the sector table is transferred during format commands. All transfers are high-speed 16-bit I/O operations except for Error Correction Code (ECC) bytes transferred during Read/Write Long commands.

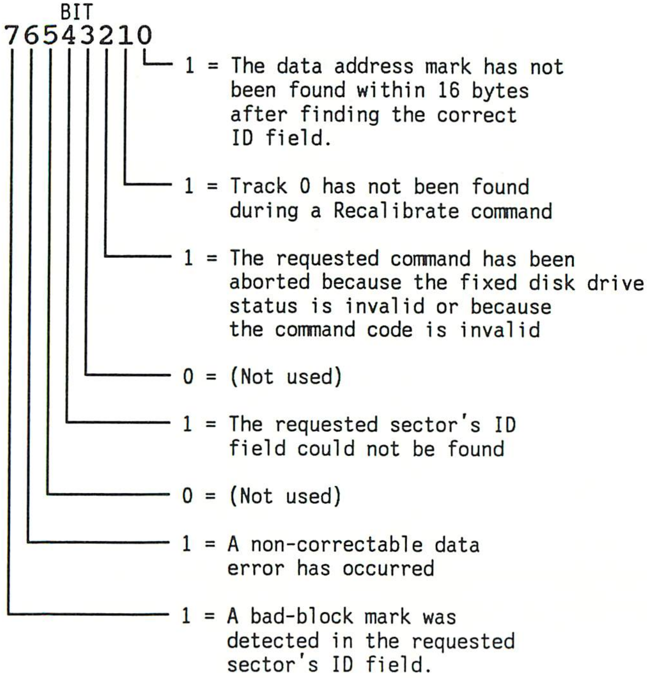
ERROR (1F1h, READ ONLY)

The Error register contains error status from the last command executed by the fixed disk drive controller. The contents of this register are valid:

- When the error bit (ER) is set in the status register
- When the fixed disk drive controller has completed execution of its internal diagnostics.

The contents of the Error register are interpreted as a diagnostic status byte after the execution of a diagnostic command or when the system is initialized.

The format of the Error register byte is shown below.



1 = The data address mark has not been found within 16 bytes after finding the correct ID field.

1 = Track 0 has not been found during a Recalibrate command

1 = The requested command has been aborted because the fixed disk drive status is invalid or because the command code is invalid

0 = (Not used)

1 = The requested sector's ID field could not be found

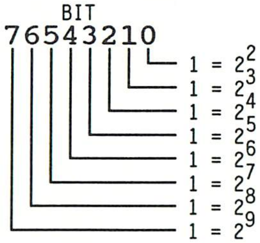
0 = (Not used)

1 = A non-correctable data error has occurred

1 = A bad-block mark was detected in the requested sector's ID field.

WRITE PRECOMPENSATION CYLINDER (1F1h, WRITE ONLY)

The Write Precompensation Cylinder register defines the cylinder on which write precompensation begins. The controller multiplies the value in the register by 4. The bits of this register have greater value, or are "weighted" more than usual (see diagram).



The following list shows some bit values and the resulting starting cylinders for write precompensation:

Bits	Starting Cylinder
00000001	4
00000010	8
00000100	16
00001000	32
00010000	64
00100000	128
01000000	256
10000000	512

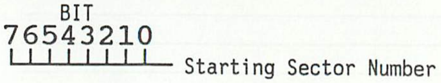
SECTOR COUNT (1F2h)

The Sector Count register defines either the number of sectors of data to be read or written, or the number of sectors per track for format commands. If the value in this register is zero, a count of 256 sectors is specified. The sector count is decremented as each sector is read. The Sector Count register contains the number of sectors left to access when an error occurs in a multi-sector operation.

During the Initialize Drive Parameters command, the Sector Count register contains the number of sectors per track.

SECTOR NUMBER (1F3h)

The Sector Number register contains the starting sector number for any fixed disk drive access.

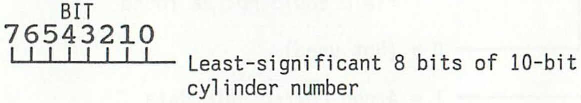


CYLINDER-LOW AND CYLINDER-HIGH (1F4h AND 1F5h)

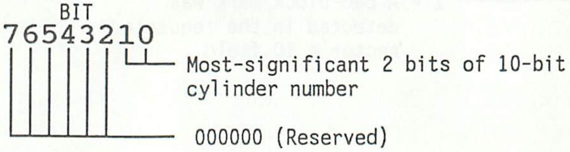
The Cylinder-Low and Cylinder-High registers contain the starting cylinder number for any fixed disk drive access.

The Cylinder-Low register is for the least-significant 8 bits of the 10-bit cylinder number. The two most-significant bits of the cylinder number should be loaded into the Cylinder-High register, bits 0, and 1. Bit 1 of the Cylinder-High register is the most-significant bit of the 10-bit cylinder address. At the completion of a command, these registers are updated to reflect the current position of the heads.

Cylinder-Low Register:



Cylinder-High Register:



SECTOR SIZE/DRIVE/HEAD (1F6h)

This register contains the parameters defined below:

```
    BIT
76543210
| || └┴┴┴─── = Head-Select Number
| ||            0000 = 0     1000 = 8
| ||            0001 = 1     1001 = 9
| ||            0010 = 2     1010 = 10
| ||            0011 = 3     1011 = 11
| ||            0100 = 4     1100 = 12
| ||            0111 = 5     1101 = 13
| ||            0110 = 6     1110 = 14
| ||            0111 = 7     1111 = 15
| ||
| |└──────── 0 = Select Fixed Disk Drive 1
| |          1 = Select Fixed Disk Drive 2
| |
| └┴──────── Sector Size
|            00 = Reserved
|            01 = 512 bytes/sector
|            10 = Reserved
|            11 = Reserved
|
└─────────── 1 = Use ECC for the data fields
```

STATUS (1F7h, READ ONLY)

This register contains the fixed disk drive controller and fixed disk drive status. The contents of this register are updated at the completion of each command. If the Busy bit is set, no other bits are valid. Reading this register clears the hardware interrupt line, IRQ14.

BIT
76543210

1 = Error has been detected. Examine Error Register and the other bits in this register to determine the source.

1 = Drive's INDEX- signal is active.

1 = A correctable data error has occurred and has been corrected. This condition will not terminate a multi-sector read operation.

1 = Data request--the controller is ready for a byte- or word-length data transfer. Verify the state of this bit before a data transfer.

1 = Drive's SEEK COMPLETE- signal is active (See Note)

1 = Drive's WRITE FAULT- signal is active (See Note)

1 = Drive's READY- signal is active (See Note)

1 = Controller is busy executing a command. Other fixed disk drive controller register's contents may not be valid until this bit is reset (=0).

Note: When an error exists, the state of the signals does not change until the error is read by the system.

COMMAND (1F7h, WRITE ONLY)

Fixed disk drive controller commands are written to the Command register. The following is a list of executable commands, command codes, and necessary command parameters.

Bit								
7	6	5	4	3	2	1	0	Command Name
1	0	0	1	0	0	0	1	Initialize Drive Parameters
0	1	1	1	S	S	S	S	Seek (Note 1)
0	0	0	1	S	S	S	S	Recalibrate (Note 1)
0	0	1	0	0	0	L	R	Read Sectors (Notes 2 and 3)
0	0	1	1	0	0	L	R	Write Sectors (Notes 2 and 3)
0	1	0	0	0	0	0	R	Verify Sectors (Note 3)
0	1	0	1	0	0	0	0	Format Track
1	0	0	1	0	0	0	0	Execute Controller Diagnostics
1	1	1	0	1	1	0	0	Identify (Note 4)
1	1	1	0	0	1	0	0	Read Sector Buffer (Note 4)
1	1	1	0	1	0	0	0	Write Sector Buffer (Note 4)

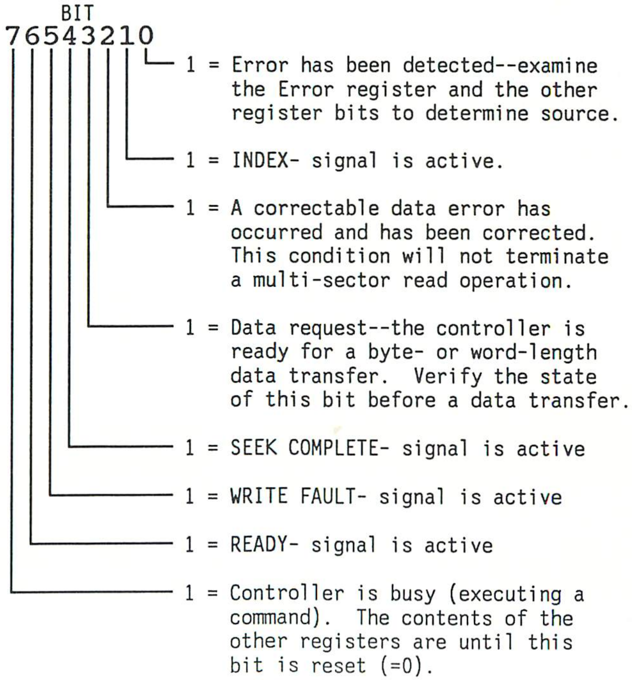
Notes: 1. S S S S = Step rate code (use following table).

0000	35 us	1000	4.0 ms
0001	0.5 ms	1001	4.5 ms
0010	1.0 ms	1010	5.0 ms
0011	1.5 ms	1011	5.5 ms
0100	2.0 ms	1100	6.0 ms
0101	2.5 ms	1101	6.5 ms
0110	3.0 ms	1110	3.2 us
0111	3.5 ms	1111	16 us

2. If L = 0, Read or Write is performed.
If L = 1, Read Long or Write Long is performed.
3. If R = 0, Retries are enabled.
If R = 1, Retries are disabled.
4. The 40-MB drive does not support the Identify, Read Sector Buffer, or Write Sector Buffer commands.

ALTERNATE STATUS (3F6h, READ ONLY)

The contents of this register are similar to those of the Status register, except in the timing and latch control of the specified signals. Reading this register does not clear any hardware conditions.



1 = Error has been detected--examine the Error register and the other register bits to determine source.

1 = INDEX- signal is active.

1 = A correctable data error has occurred and has been corrected. This condition will not terminate a multi-sector read operation.

1 = Data request--the controller is ready for a byte- or word-length data transfer. Verify the state of this bit before a data transfer.

1 = SEEK COMPLETE- signal is active

1 = WRITE FAULT- signal is active

1 = READY- signal is active

1 = Controller is busy (executing a command). The contents of the other registers are until this bit is reset (=0).

DRIVE CONTROL (3F6h, WRITE ONLY)

The Drive Control register defines several functions of the fixed disk drive controller.

BIT
76543210

0 (Not used)

0 = Enables interrupts
1 = Disables interrupts

1 = Resets controller

0 = Disables head select bit 3
1 = Enables head select bit 3

0000 (Not used)

DRIVE ADDRESS (3F7h, READ ONLY)

This register loops back the drive select and head select addresses of the most recently selected fixed disk drive. The bits in this port are as follows:

BIT
76543210

0 = Drive 1 selected

0 = Drive 2 selected

Head select

0000 = 15 1000 = 7
0001 = 14 1001 = 6
0010 = 13 1010 = 5
0011 = 12 1011 = 4
0100 = 11 1100 = 3
0101 = 10 1101 = 2
0110 = 9 1110 = 1
0111 = 8 1111 = 0

0 = Drive's WRITE GATE- signal is active (low).

Reserved for use by the multipurpose controller

Commands

Commands are issued to the controller by loading the pertinent registers with the needed parameters, enabling the fixed disk drive controller interrupt, and then writing the command code to the command register. Command execution begins when a command is written to the Command register.

Table 9-3 lists the fixed disk drive controller commands.

Table 9-3. Fixed Disk Drive Controller Commands

Initialize Drive Parameters
Seek
Recalibrate
Read Sectors
Read Long
Write Sectors
Write Long
Verify Sectors
Format Sectors
Execute Controller Diagnostic
Identify
Read Buffer
Write Buffer

INITIALIZE DRIVE PARAMETERS

The Initialize Drive Parameters command enables the host to configure the controller to work with fixed disk drives that have different capacities and characteristics. Fixed disk drives 1 and 2 may be initialized for different drive parameters.

The Sector Size/Drive/Head Register must contain the maximum head number. The Sector Count register must contain the the maximum sectors per track prior to executing this command.

The parameters loaded into the register prior to issuance of the command define the drive configuration for the specified fixed disk drive. If the Initialize Drive Parameters command is not issued, the fixed disk drive controller will default to 17 sectors per track and 4 heads.

SEEK

The Seek command initiates a Seek to the track and selects the head specified. The fixed disk drive need not be formatted for a seek to execute properly. The controller supports buffered step seeks, allowing overlapped seeks on the drives.

After initiating a Seek on one fixed disk drive, another command can be issued to the other drive. If a new command is received for a fixed disk drive with an outstanding Seek, then the controller waits, with BUSY active, for the Seek to complete before executing the new command. There is no timeout condition in the controller while waiting for buffered-step seeks to complete.

RECALIBRATE

The Recalibrate command moves the read/write heads to cylinder 0. If the fixed disk drive is unable to reach cylinder 0, the command is aborted with the error bit set in the Status Register and the Track 0 bit set in the Error Register.

The stepping-rate code included with this command does not have any effect on the recalibrate stepping, but is used as the stepping rate for any subsequent implied seeks executed by the controller.

READ SECTORS

The Read Sectors command reads from 1 to 256 sectors as specified in the Sector Count register, beginning at the specified sector. If the fixed disk drive is not already on the requested track, an implied seek is performed at the stepping rate defined in the last Recalibrate command.

After reaching the specified track, the controller begins searching for the appropriate ID field. If retries are disabled, a maximum of 2 revolutions are taken and if retries are enabled, 16 revolutions are taken before reporting an ID Not Found error. If the ID is read correctly, the data address mark must be recognized in 16 bytes, or the Data Address Mark Not Found error will be reported.

After the data address mark is found, the data field is read, and the sector read is finished with either no error, a correctable data error, or a non-correctable data error, depending on whether or not the ECC bytes are correct for the preceding data field.

If an error occurs during a multiple-sector read, the read terminates at the sector where the error occurs. The system may then read the registers, determine what error has occurred, and on which sector. If the error was a non-correctable data error, the flawed data is still returned to the system.

READ LONG

A Read Long command returns the data field and the ECC bytes contained in the data field of the desired sector.

During a Read Long operation, the controller does not check the ECC bytes to determine if there has been any type of data error. The data bytes are read out of the sector buffer at the completion of the command, which is signaled by an interrupt. All data transfers are high-speed 16-bit operations and all ECC byte transfers on Read Long commands are slower 8-bit operations. The 40-MB fixed disk has 4 ECC bytes and the 130-MB drive/controller has 7 ECC bytes.

WRITE SECTORS

The Write Sectors command writes from 1 to 256 sectors of data, as specified in the Sector Count register, beginning at the specified sector. If the fixed disk drive is not already on the requested track, an implied seek is performed at the stepping rate defined in the last Recalibrate command.

Once at the desired track, the controller begins searching for the appropriate ID field. If retries are disabled, a maximum of two revolutions will be taken and if retries are enabled, 16 revolutions will be taken before reporting an ID Not Found error. If the ID is read correctly, the data loaded in the sector buffer is written to the data field of the sector, along with a 4-byte ECC. If an error occurs during a multiple-sector write, the write terminates at the sector where the error occurs. The system may then read the registers, determine what error has occurred, and on which sector.

WRITE LONG

A Write Long operation may be executed by setting the long bit in the command code. The Write Long command writes the data field and the ECC bytes directly from the sector buffer; the controller does not generate the ECC bytes. All data transfers are high-speed 16-bit operations and all ECC byte transfers on Write Long commands are slower 8-bit operations. The 40-MB fixed disk has 4 ECC bytes and the 130-MB drive/controller has 7 ECC bytes.

VERIFY SECTORS

This command is identical to the Read Sectors command, except that no data is transferred back to the system and no Read Long operations are permitted. The read procedure described in the Read command is followed and any errors encountered are reported to the system.

FORMAT TRACK

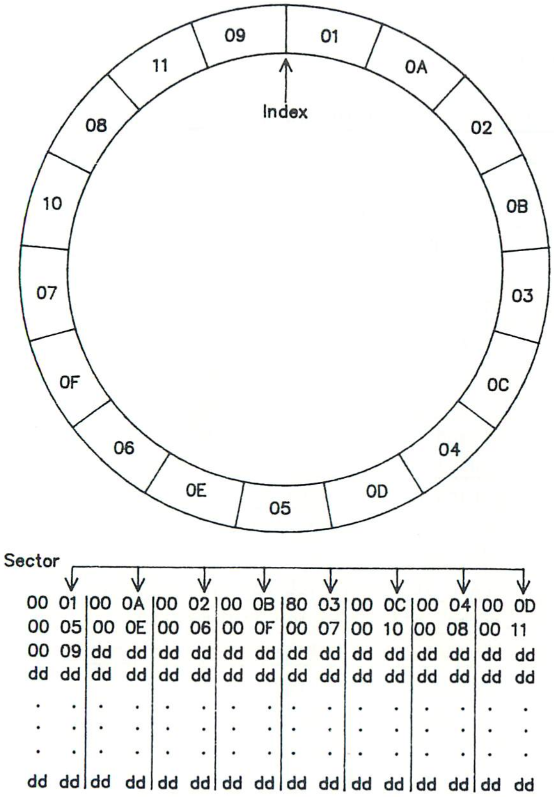
The Format Track command formats the track specified in the Data register. If the fixed disk drive is not already on the specified track, an implied Seek is performed at the stepping rate defined in the last Recalibrate command. After reaching the specified track, the ID and data fields are written using the sector table in the sector buffer.

The sector table contains 2 bytes per sector on the track. The first byte is 00h if the sector is to be formatted normally, or 80h if the sector is to be formatted bad. The second byte is the logical sector number of the sector.

As soon as the fixed disk drive controller senses the index pulse from the fixed disk drive, formatting begins by writing the first physical sector with the logical sector number in the first entry of the sector table.

Subsequent physical sectors are formatted in turn from the sector table. The order of the sector table entries will correspond to the interleave factor of the track. Media defects may be marked bad on a sector level, allowing the remainder of the track to be used.

The sector table should be written into the sector buffer prior to issuance of the command, and additional bytes should be loaded into the buffer until it is full (512 bytes). Figure 9-1 shows the contents of a typical sector table for a 17-sector track with an interleave factor of 2 and sector 3 marked bad.



```
00 01 |00 0A |00 02 |00 0B |80 03 |00 0C |00 04 |00 0D
00 05 |00 0E |00 06 |00 0F |00 07 |00 10 |00 08 |00 11
00 09 |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd
dd dd |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd
 .  . | .  . | .  . | .  . | .  . | .  . | .  . | .  .
 .  . | .  . | .  . | .  . | .  . | .  . | .  . | .  .
 .  . | .  . | .  . | .  . | .  . | .  . | .  . | .  .
dd dd |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd |dd dd
```

Note: "dd" is a "don't care" byte used to make up a total of 512 bytes.

Figure 9-1. Typical Sector Table

EXECUTE CONTROLLER DIAGNOSTIC

This command performs the internal diagnostic tests implemented by the controller. The results of the test are reported to the Error register immediately after execution of the command. The value in the Error register should be viewed as an unique 8-bit code and not as the single-bit flags previously defined.

Table 9-4 lists the error codes and the corresponding explanation.

Table 9-4. Fixed Disk Drive Controller Error Codes

Error Code	Description
01h	No error detected
02h	Unidentified controller error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
06h	Host interface device error
07h	Format error
08h	ESDI communications error

IDENTIFY

The Identify command allows the host to receive parameter information from the drive. When the command is issued, the controller gets the parameters from the drive, stores them in the sector buffer, sets the DRQ bit in the status register, and waits for the host to read the information out of the sector buffer. The parameter words in the buffer are described in Table 9-5.

Table 9-5. ESDI Parameter Words

Word	Contents
Word 0	General configuration
Word 1	Number of fixed cylinders
Word 2	Reserved
Word 3	Number of heads
Word 4	Number of unformatted bytes per physical track
Word 5	Number of unformatted bytes per sector
Word 6	Number of physical sectors per track
Word 7	Number of bytes in the inter-sector gaps
Word 8	Number of bytes in the sync fields
Word 9 . . .	
Word 255	Reserved

Table 9-6 gives bit definitions of the general configuration word.

Table 9-6. Configuration Word Bits

Bit 0	Reserved
Bit 1	1=Hard sectored
Bit 2	1=Soft sectored
Bit 3	1=Not MFM encoded
Bit 4	1=Head switch time greater than 15 us
Bit 5	1=Spindle motor control option implemented
Bit 6	1=Fixed drive
Bit 7	1=Removable cartridge drive
Bit 8	1=Transfer rate less than or equal to 5 mb/s
Bit 9	1=Transfer rate greater than 5 mb/s but less than or equal to 10 mb/s
Bit 10	1=Transfer rate greater than 10 mb/s
Bit 11	1=Rotational speed tolerance is greater than 0.5 percent
Bit 12	1=Data strobe offset option implemented
Bit 13	1=Track offset option implemented
Bit 14	1=Format speed tolerance gap required
Bit 15	0=Magnetic disk drive 1=Nonmagnetic disk drive

READ BUFFER

The Read Buffer command allows the host to read the current contents of the controller's sector buffer. When this command is issued, the controller goes busy, sets up the sector buffer for a read operation, sets the data request bit (DRQ), and goes not busy. The host can then read up to 512 bytes of data.

WRITE BUFFER

The Write Buffer command allows the host to overwrite the contents of the controller's sector buffer with any data pattern desired. When this command is issued, the controller goes busy, sets up the sector buffer for a write operation, sets the data request bit (DRQ), and goes busy. The host can then write up to 512 bytes of data.

Fixed Disk Drive Controller Error Reporting

The errors that are valid for each command are defined in the matrix below:

	BB	UD	ID	AC	TZ	AM	NR	WF	SC	CD	ER
Init Drive Parms							V	V	V		
Seek			V	V			V	V	V		V
Recalibrate				V	V		V	V	V		V
Read Sector	V	V	V	V		V	V	V	V	V	V
Read Long	V		V	V		V	V	V	V		V
Write Sector	V		V	V			V	V	V		V
Write Long	V		V	V			V	V	V		V
Verify Sector	V	V	V	V		V	V	V	V	V	V
Format Track			V	V			V	V	V		V
Cntlr Diagnostic											V
Invalid CMD Code				V							V

BB = Bad block detected
UD = An uncorrectable data error
ID = Requested ID not found
AC = An aborted command error
TZ = Track 0 not found error
AM = Data Address Mark not found
NR = Disk drive not ready detected
WF = Disk drive write fault detected
SC = Disk drive seek complete not detected
CD = A corrected data error
ER = The error bit in the Status register
V = Indicates that this error type is valid for this command

9.2 40-MB FIXED DISK DRIVE SYSTEM

The 40-MB fixed disk drive system provides 40-MB of data storage on a half-height, fixed disk drive. This system:

- Has the fixed disk drive controller integrated into the fixed disk drive assembly.
- Connects to a host adapter on the multipurpose controller for data and decoded I/O-select lines.
- Frees an additional expansion slot by eliminating the need for a separate fixed disk drive controller.

Figure 9-2 shows the 40-MB fixed disk drive for the COMPAQ DESKPRO 386.

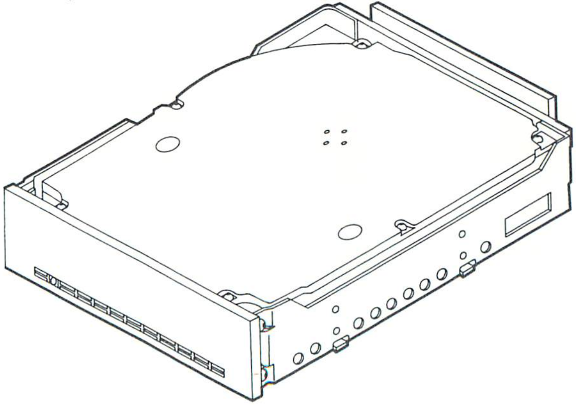


Figure 9-2. 40-MB Fixed Disk Drive

Figure 9-3 shows the functional block diagram of the 40-MB fixed disk drive system.

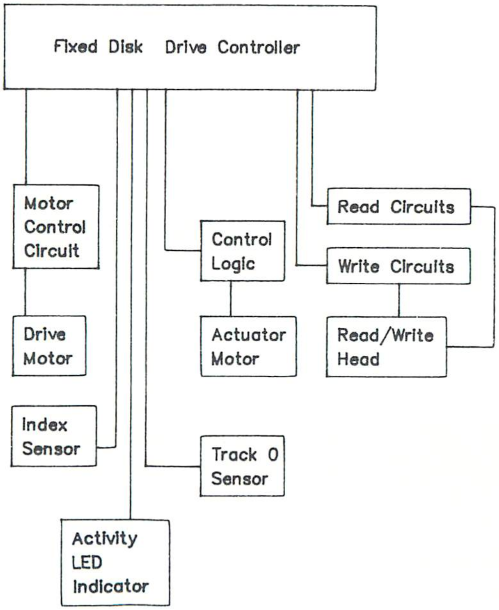


Figure 9-3. 40-MB Fixed Disk Drive System Functional Block Diagram

Specifications

Table 9-7 lists the fixed disk drive physical and electrical specifications.

Table 9-7. 40-MB Fixed Disk Drive Physical and Electrical Specifications

Capacity:	
Unformatted	51.0 MB
Formatted	42.6 MB
Access time:	
Track-to-track	8 ms
Average	29 ms
Maximum	70 ms
Drive type (used in SETUP program)	17
Data-transfer rate (mb/s	5.0
Rotational speed (RPM)	3600
Number of heads	5
Number of platters	3
Number of cylinders	980
Write precompensation cylinder	128
Landing zone cylinder	980
Size:	
Width (in. (mm))	5.75 (146)
Height (in. (mm))	1.625 (41.3)
Depth (in. (mm))	8.8 (223.5)
Weight (lb (kg))	4 (1.8 kg)
Number of ECC bytes	4

Configuring the 40-MB Fixed Disk Drive System

Two 40-MB fixed disk drive systems can be installed in a COMPAQ DESKPRO 386.

The fixed disk drive controller is an integral part of the 40-MB fixed disk drive system. To allow more than one fixed disk drive controller to work using the same I/O addresses, the fixed disk drive controllers were designed to respond only to commands to drive C or drive D, as specified by a jumper. The configuration jumper is shown in Figure 9-4.

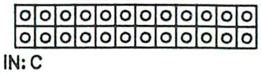


Figure 9-4. Configuration Jumper on a 40-MB Fixed Disk Drive

Both fixed disk drive systems connect in a daisy-chain manner to the multipurpose controller. The system turns on the fixed disk drive systems sequentially (one after the other) to prevent excessive current draw on the power supply.

The 40-MB fixed disk drive does not support the Identify, Read Sector Buffer, or Write Sector Buffer commands.

There are no terminating resistor packs on the 40-MB fixed disk drives. The presence of a configuration jumper designates the drive as C:. The absence of the jumper designates the drive as D:.

Figure 9-5 shows an interconnection diagram for the COMPAQ DESKPRO 386 with two 40-MB fixed disk drive systems.

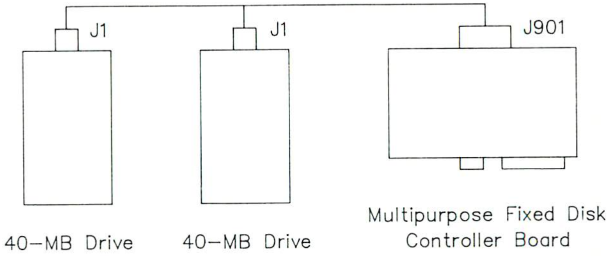


Figure 9-5. Interconnection Diagram for a Dual 40-MB Fixed Disk Drive System

Connectors

Connector J1 is connected to the multipurpose controller board using a 40-conductor cable. This connection supplies control and data signals to the fixed disk drive system.

Connector J2 is connected to the system board, using a 4-conductor cable. This connection supplies power to the fixed disk drive system.

Table 9-8 describes the signals for connector J1. Figures 9-6 and 9-7 show both connectors J1 and J2..

Table 9-8. J1, Fixed Disk Drive Host-Adapter Connector Signal Descriptions

Signal	Pin	I/O	Description
SLAVE PRESENT-	39	O	Active-low signal indicating to the host that a second drive is present.
CS1FX-	37	I	Chip select 1Fxh. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 1F0h and 1F7h.
CS3FX-	38	I	Chip select 3Fxh. Chip select decoded from the address bus and gated with AEN to select the controller registers at addresses 3F6h through 3F7h.
DA0 DA1 DA2	35 33 36	I	Address lines A2-A0. Buffered address lines from the address bus to the fixed disk drive controller.
DALE	28	I	Address latch enable. Signals that address bus signals are stable and valid.
DD7 DD6 DD5 DD4 DD3 DD2 DD1 DD0	3 5 7 9 11 13 15 17	I I I I I I I I	Data bit 0-7. Least-significant eight bits of the 16-bit data bus for data and status communication between the controller and the host. D7 is the most-significant bit of this byte.

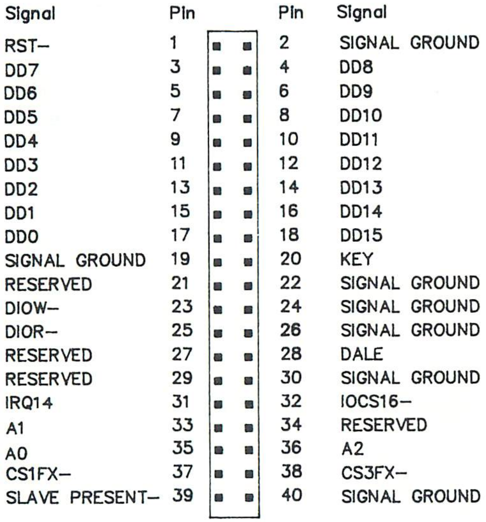
Note: Pins 20, 21, 27, and 29 are not connected.

(Continued)

Table 9-8. J1, Fixed Disk Drive Host-Adapter Connector Signal Descriptions (Concluded)

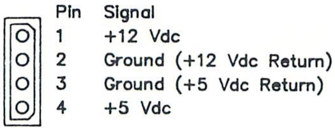
Signal	Pin	I/O	Description
DD8	4	I	Data bit 8-15. Most-significant eight bits for data and status communication between the controller and the host. DD15 is the most-significant bit of this byte.
DD9	6	I	
DD10	8	I	
DD11	10	I	
DD12	12	I	
DD13	14	I	
DD14	16	I	
DD15	18	I	
DIOW-	23	I	I/O write. Active when the host writes a control byte or data word to the controller
DIOR-	25	O	I/O read. Active when the host reads a status byte or data word to the controller.
IO16CS-	32	I	Chip select used to signal the processor that the current I/O cycle is a 16-bit, single wait-state cycle.
IRQ14	31	O	Interrupt request 14. Asserted by the controller to interrupt the processor upon completion of a fixed disk operation.
RST-	1	I	Reset. This signal resets the controller to the initial power-on condition
PDIAG	34	I/O	Signal from drive D: (if installed) to drive C: indicating that it has passed the diagnostic command.
SIGNAL GROUND	2,19, 22,24, 26,30,40	-	Return conductor

Note: Pins 20, 21, 27, and 29 are not connected.



Signal	Pin	Pin	Signal
RST–	1	2	SIGNAL GROUND
DD7	3	4	DD8
DD6	5	6	DD9
DD5	7	8	DD10
DD4	9	10	DD11
DD3	11	12	DD12
DD2	13	14	DD13
DD1	15	16	DD14
DD0	17	18	DD15
SIGNAL GROUND	19	20	KEY
RESERVED	21	22	SIGNAL GROUND
DIOW–	23	24	SIGNAL GROUND
DIOR–	25	26	SIGNAL GROUND
RESERVED	27	28	DALE
RESERVED	29	30	SIGNAL GROUND
IRQ14	31	32	IOCS16–
A1	33	34	RESERVED
A0	35	36	A2
CS1FX–	37	38	CS3FX–
SLAVE PRESENT–	39	40	SIGNAL GROUND

Figure 9-6. J1, 40-MB Fixed Disk Drive Host Adapter Connector



Pin	Signal
1	+12 Vdc
2	Ground (+12 Vdc Return)
3	Ground (+5 Vdc Return)
4	+5 Vdc

Figure 9-7. J2, 40-MB Fixed Disk Drive Power Connector

9.3 130-MB FIXED DISK DRIVE SYSTEM

The 130-MB fixed disk drive system provides 130-MB of data storage on a full-height, fixed disk drive. This system:

- Uses an ESDI-type fixed disk drive controller in a 16-bit expansion slot on the system board (typically slot 6).
- Provides a data transfer rate of 10 mb/s--twice the speed of fixed disk drive systems using the ST506 standard.

130-MB Fixed Disk Drive

The 130-MB fixed disk drive is a high-capacity, high-speed, full-height, ESDI-compatible fixed disk drive. Figure 9-8 shows the 130-MB fixed disk drive for the COMPAQ DESKPRO 386.

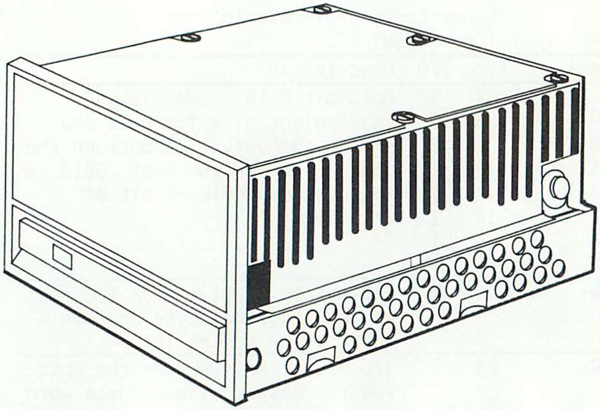


Figure 9-8. 130-MB Fixed Disk Drive

Figure 9-9 shows the functional block diagram for the 130-MB fixed disk drive.

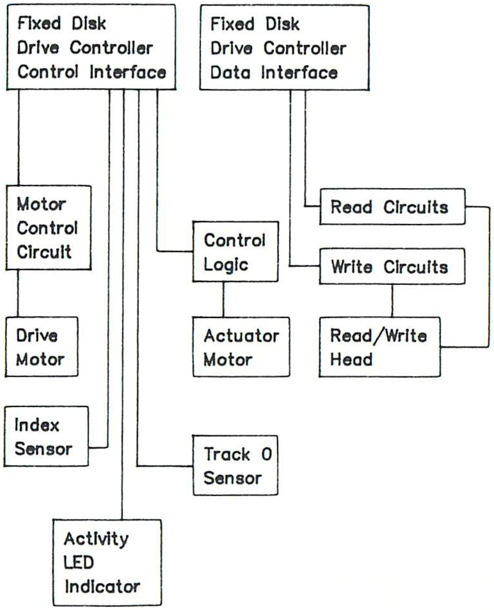


Figure 9-9. 130-MB Fixed Disk Drive Functional Block Diagram

Logical Configuration

The 130-MB fixed disk drive is an ESDI-type drive, which has an "intelligent" drive interface. The drive logic board contains circuitry normally found on a fixed disk drive controller.

Most fixed disk drives contain 17 sectors of data per track. The 130-MB fixed disk drive has 35 sectors per track. One of these sectors is reserved for error management--when a sector is detected as bad, the system reassigns the reserved sector to replace the bad sector.

Since most operating systems are not adapted to a 34-sector arrangement, the 130-MB fixed disk drive system has a Translate mode to rearrange the logical configuration of the drive. In the Translate mode, as drive type 25, the drive appears to have 17 sectors per track instead of 34, and 16 heads instead of 8.

Specifications

Table 9-9 lists the physical description of the 130-MB fixed disk drive.

Table 9-9. 130-MB Fixed Disk Drive Physical and Electrical Specifications

Capacity:	
Unformatted	161.8 MB
Formatted	134.5 MB
Access Time:	
Track-to-track	5 ms
Average	<25 ms
Maximum	50 ms
Drive type (used in SETUP program)	25
Data-transfer rate (mb/s)	10.0
Rotational speed (RPM)	3600
Number of physical heads	8
Number of logical heads	16
Physical sectors/track	34
Logical sectors/track	17
Number of platters	5
Number of cylinders	966
Landing zone cylinder	966
Write precompensation cylinder	Not used
Size:	
Width (in. (mm))	5.75 (146)
Height (in. (mm))	3.25 (83)
Depth (in. (mm))	8.0 (203)
Weight (lb (kg))	7.5 (3.4)
Number of ECC bytes	7

Configuring the 130-MB Fixed Disk Drive System

The fixed disk drive should have its drive-select jumpers set to DS1. A terminating resistor pack is installed on the fixed disk drive of a single fixed disk drive system, which is all that is allowed.

Figure 9-10 shows an interconnection diagram for the 130-MB fixed disk drive system.

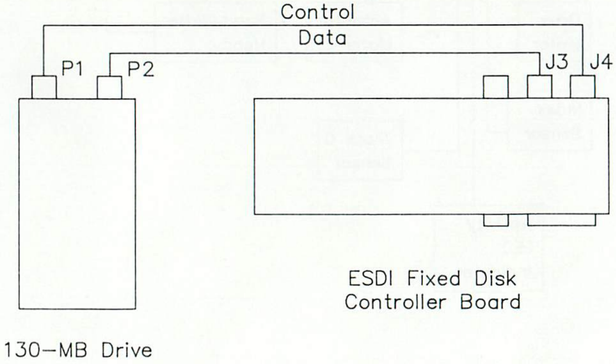


Figure 9-10. 130-MB Fixed Disk Drive System Interconnection Diagram

Jumpers

Table 9-10 lists the fixed disk drive controller jumpers. The jumpers on the controller are shown in Figure 9-11, which appears in the following section.

Table 9-10. Fixed Disk Drive Controller Jumpers

Jumper	Function	
W3	Fixed Disk Drive Base Address Select. This address selection is available only for special circumstances and under normal circumstances should never be changed.	
	No jumper or W3,2-3	Standard Address Select (1F0h, standard setting)
	(W3,2-3)	Alternate Address Select (170h)

The absence or presence of jumper W2 selects the Translate mode for the fixed disk drive. In the Translate mode, the fixed disk drive controller changes the logical arrangement of the data on the fixed disk drive so that the fixed disk drive appears to have 17 sectors per track and 16 heads. The absence of jumper W2 selects the Translate mode.

COMPAQ ESDI Fixed Disk Drive Controller

The COMPAQ ESDI fixed disk drive controller is compatible with the ESDI standard that specifies signal, connectors, and command protocols.

The ESDI controller:

- Provides for the control of the 130-MB fixed disk drive
- Plugs directly into a 16-bit expansion slot
- Incorporates a 56-bit Error Correction Code (ECC) polynomial for error detection and correction
- Has on-board diagnostics

Figure 9-11 shows the ESDI controller.

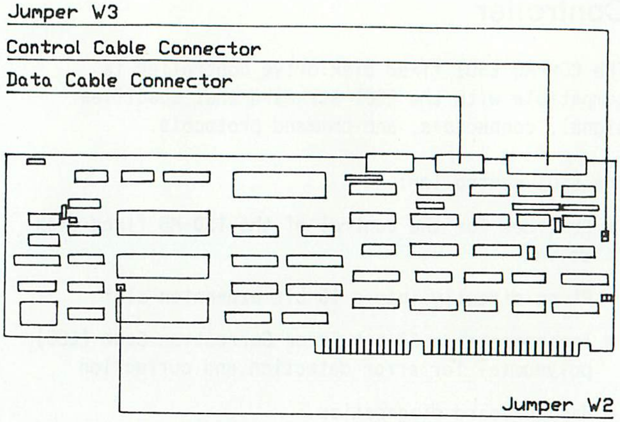


Figure 9-11. COMPAQ ESDI Fixed Disk Drive Controller

Figure 9-12 shows the pinout of J3, the data cable connector, and Figure 9-13 shows J4, the control cable connector.

Signal	Pin	Pin	Signal
–DRIVE SELECTED	1	2	–SECTOR
–COMMAND COMPLETE	3	4	–ADDRESS MARK ENABLE
SIGNAL GROUND	5	6	SIGNAL GROUND
+WRITE CLOCK	7	8	–WRITE CLOCK
SIGNAL GROUND	9	10	+READ/REFERENCE CLOCK
–READ/REFERENCE CLOCK	11	12	SIGNAL GROUND
+NRZ WRITE DATA	13	14	–NRZ WRITE DATA
SIGNAL GROUND	15	16	SIGNAL GROUND
+NRZ READ DATA	17	18	–NRZ READ DATA
SIGNAL GROUND	19	20	–INDEX

Figure 9-12. J3, Data Cable Connector

Signal	Pin	Pin	Signal
GROUND	1	2	HEAD SELECT 2^3–
	3	4	HEAD SELECT 2^2–
	5	6	WRITE GATE–
	7	8	CONFIG/STATUS DATA–
	9	10	TRANSFER ACK–
	11	12	ATTENTION–
	13	14	HEAD SELECT 2^0–
	15	16	SECTOR–
	17	18	HEAD SELECT 2^1–
	19	20	INDEX–
	21	22	READY–
	23	24	TRANSFER REQ–
	25	26	DRIVE SELECT 1–
	27	28	DRIVE SELECT 2–
	29	30	RESERVED
	31	32	READ GATE–
	33	34	COMMAND DATA–

Figure 9-13. J4, Control Cable Connector

Figure 9-14 shows the functional block diagram for the ESDI controller.

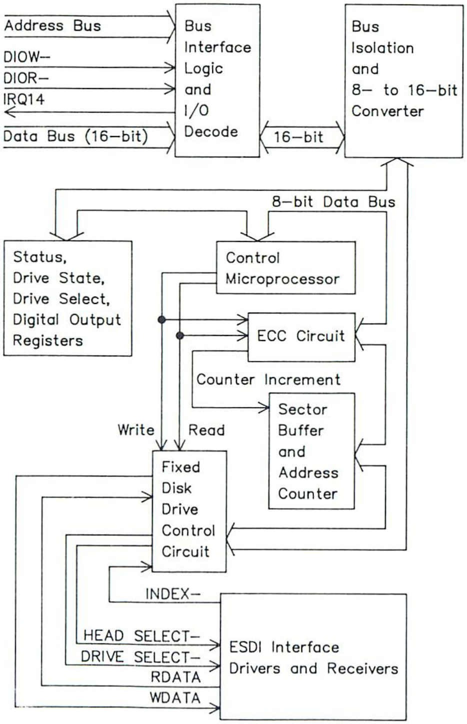

Address Bus
DIOW–
DIOR–
IRQ14
Data Bus (16–bit)
Bus Interface Logic and I/O Decode
16–bit
Bus Isolation and 8– to 16–bit Converter
8–bit Data Bus
Status, Drive State, Drive Select, Digital Output Registers
Control Microprocessor
ECC Circuit
Counter Increment
Sector Buffer and Address Counter
Write
Read
Fixed Disk Drive Control Circuit
INDEX–
HEAD SELECT–
DRIVE SELECT–
RDATA
WDATA
ESDI Interface Drivers and Receivers

Figure 9-14. COMPAQ ESDI Fixed Disk Drive Controller Functional Block Diagram

ESDI Controller Commands

The ESDI controller is compatible with all software written for the ST506-compatible fixed disk drive controller.

The ESDI controller supports all the commands listed in the section entitled "Fixed Disk Drive Programming" earlier in this chapter.

For the ESDI controller, the Write Precompensation Cylinder register (I/O address 1F1h) is reserved. The ESDI interface does not use write precompensation.

For the Seek and Recalibrate commands, the step rate codes are ignored on the 130-MB controller.

Connectors

Table 9-11 describes the 34-pin control cable connector pinouts and signal descriptions. Table 9-12 describes the 20-pin data cable connector pinouts and signal descriptions. All I/O designations are with respect to the drive.

Table 9-11. 34-Pin Control Cable Connector Description

Signal Name	Pin	I/O	Description
HEAD SELECT 2^3- 2^2- 2^0- 2^1-	2 4 14 18	I	Lines that allow selecting individual read/write heads in a binary code sequence.
WRITE GATE-	6	I	Signal allows data to be written on the disk.
CONFIG/STATUS DATA-	8	O	Drive presents serial data on this line upon request from the controller.
TRANSFER ACK-	10	O	Line from the drive indicating that a transfer request has been acknowledged and valid data transferred. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-.
ATTENTION-	12	O	Signal from the drive indicating the drive wants the controller to request its status.
SECTOR-	16	O	Indicates the beginning of a sector.
INDEX-	20	O	Indicates the beginning of a track
READY-	22	O	Signal indicates only that the spindle is up to speed.
TRANSFER REQ-	24	I	Line from the controller requesting that one bit of data be sent between the drive and the controller. All transfers handshake with TRANSFER REQ- and TRANSFER ACK-.
DRIVE SELECT 1- DRIVE SELECT 2-	26 28	I	These bits provide the binary-coded drive select address.
READ GATE-	32	I	Signal allows data to be read from the disk.
COMMAND DATA	34	I	When a command is issued, 16 information bits of serial data, plus parity, are sent to the drive on this line.
RESERVED	30		

Note: All odd numbered pins are ground.

Table 9-12. 20-Pin Data Cable Connector Description

Signal	Pin	I/O	Description
DRIVE SELECTED-	1	O	A status line provided to inform the controller system of the selection status of the drive.
SECTOR-	2	O	Indicates the beginning of a sector.
COMMAND COMPLETE-	3	O	A status line that indicates command completion to the controller.
ADDRESS MARK ENABLE-	4	O	The trailing edge of this signal with the WRITE GATE- asserted initiates writing the sync field on the drive.
+READ/REFERENCE CLOCK -READ/REFERENCE CLOCK	10 11	O	Differential clock signal used for reading data bits from the drive.
+NRZ WRITE DATA -NRZ WRITE DATA	13 14	I	A differential pair that defines the data to be written on the track.
+NRZ READ DATA -NRZ READ DATA	17 18	O	Data recovered by reading previously written information is transmitted to the controller via this differential pair.
+WRITE CLOCK -WRITE CLOCK	7 8	I	A differential pair of clocks used for writing data bits to the drive.
INDEX	20	O	Indicates the beginning of a track.
GROUND	5, 6, 7 12, 15, 16 19		

Chapter 10

FIXED DISK DRIVE BACK-UP SYSTEM

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Chapter 10
FIXED DISK DRIVE BACK-UP SYSTEM

10.1 INTRODUCTION

The 40-MB Fixed Disk Drive Back-up system uses a 3M DC2000 tape cartridge or equivalent and the COMPAQ MS-DOS COMPAQ TAPE Utility Version 2 (or later) to provide a data back-up for fixed disk drives. The 40-MB Fixed Disk Drive Back-up stores a maximum of 40 MB on a single tape cartridge.

The fixed disk drive back-up connects to the multipurpose fixed disk controller in a daisy-chain manner, along with the diskette drives. The 765 diskette controller on the multipurpose fixed disk controller controls all fixed disk drive back-up functions and data formats.

Figure 10-1 shows the 40-MB Fixed Disk Drive Back-up.

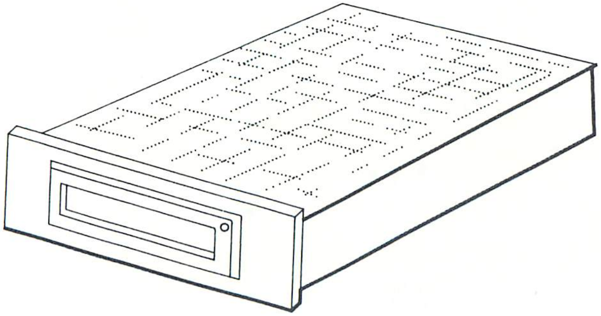


Figure 10-1. 40-MB Fixed Disk Drive Back-up
(Tape Drive)

The tape drive consists of a microprocessor, firmware, stepper motor, drive motor, read/write head, and a control logic board.

The logic board uses a Z8 microprocessor with 8 KB of ROM to control the drive. The logic board connects to the:

- Movable head, which reads and writes data
- Cartridge-installed sensor
- Write-protect sensor
- End-of-tape/beginning-of-tape (EOT/BOT) sensor
- Stepper motor, which positions the head
- Multipurpose fixed disk controller board
- DC power supply
- Drive Motor, which advances and rewinds the tape.

Figure 10-2 is a functional block diagram of the 40-MB Fixed Disk Drive Back-up.

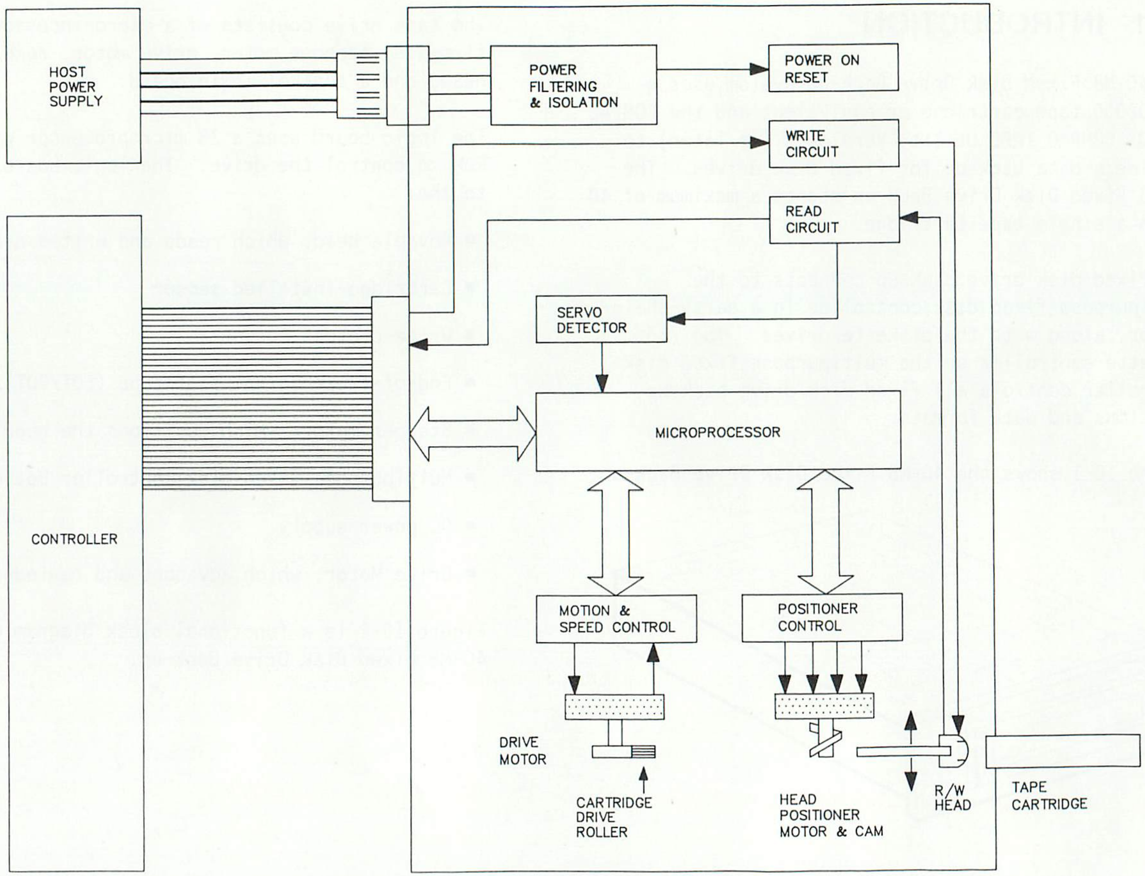


Figure 10-2. 40-MB Fixed Disk Drive Back-up (Tape Drive) Functional Block Diagram

10.2 SPECIFICATIONS

Table 10-1 lists the 40-MB Fixed Disk Drive Back-up specifications.

Table 10-1. 40-MB Fixed Disk Drive Back-up Physical and Electrical Specifications

Size:		
Width	5.65 in. (144 mm)	
Height	1.65 in. (41 mm)	
Depth	8.00 in. (203 mm)	
Weight	1.7 lb (0.77 kg)	
Formatted capacity (with ECC)	40.63 MB	
Flux reversal density	10000 FR/I	
Data-transfer rate	500 kb/s	
Head positioning time:		
Adjacent tracks	250 ms	
Move (worst case)	1 sec	
Tape speed:		
Read/write	50 in./s	
Rewind/fast forward	70 in./s	
Tape end-to-end positioning time:	DC1000 (see Note)	DC2000
Read/write	44 sec	49
Forward/reverse	31 sec	35

(continued)

Table 10-1. 40-MB Fixed Disk Drive Back-up Physical and Electrical Specifications (Concluded)

Track density	83 TPI
Number of tracks	20
Blocks/track	124
Sectors/block	18
Bytes/sector	1024

Note: DC1000 cartridges backed-up on the 10-MB Fixed Disk Drive Back-up system (supported on other COMPAQ products) can be read but not written by the 40-MB Fixed Disk Drive Back-up system.

10.3 40-MB FIXED DISK DRIVE BACK-UP COMMANDS

All fixed disk drive back-up operations are one of five fundamental processes:

1. Servo-Write, which initializes the tape media by writing indexing information.
2. Tape Format, which writes block, sector, and track information onto the tape. This information joins the indexing information previously written by Servo-Write. This process prepares data areas consistent with the NEC765 diskette controller data format.
3. Write-Data, which writes information in the same layout as standard diskette tracks.
4. Read-Data, which reads information in the same layout as diskette tracks.
5. Erase, which erases all information on tape (including servo and data).

The Servo-Write operation is initiated by executing an Enter Format Mode command followed by the Servo-Write command. This action moves the tape to the beginning, at block 0 and head 0 and then writes encoding index pulses on the tape in a streaming-write mode. These pulses are used solely by the fixed disk drive back-up and are not available to the programmer.

Note: If the Servo-Write operation is interrupted, the tape cartridge must be fully erased before it can be used again.

The format operation for tape is similar to the format process for diskette drives. To format the tape, the multipurpose fixed disk controller takes control of the interface and supplies the track and sector data for every block on the track. The data format on the tape has the characteristics of a diskette.

The 40-MB Fixed Disk Drive Back-up accepts commands from the multipurpose fixed disk controller board as pulses on the step line. The number of pulses determines the desired command. Any number of pulses not recognized as commands are ignored. The tape drive does not recognize the step pulses unless the 765 is programmed for a 3- or 6-ms gap between pulses. Table 10-2 lists the 40-MB Fixed Disk Drive Back-up commands.

Table 10-2. 40-MB Fixed Disk Drive Back-up Command Summary

Step Pulses	Command	Action
2	Stop Motion	Stops tape - deactivates BUSY- signal
3	Pause	Moves tape back two blocks - stops tape.
4	Seek Load Point	Rewinds tape at 50 IPS and goes to track 0.
5	Move Tape Forward	Moves tape forward at 70 IPS (fast forward).
6	Move Tape Back	Moves tape backward at 70 IPS (rewind).
7	Report Normal Completion	Latches BUSY- line if latest command has successfully completed.
8	Report Drive Present	Latches BUSY- line if selected.
9	Report End	Latches BUSY- line if at end of tape.
10	Report Begin	Latches BUSY- line if at tape beginning.
11	Report Cart	Latches BUSY- line if cartridge is present.
12	Report Track Found	Latches BUSY- line if track seek has completed.
13	Report New Cartridge	Latches BUSY- line if cartridge has been replaced.
14	Move Tape Against Data	Moves tape at 50 IPS (or 39 IPS if in low-density mode) toward file beginning.
15	Move Tape With Data	Moves tape at 50 IPS (or 39 IPS if in low-density mode) toward file end.
16	Enter Format Mode	Produces index pulses at end and beginning of data area to allow formatting by the 765. The drive must be in the Format mode to enable subsequent execution of the Servo Write command.
17	Enter Normal Mode	Produces index pulses at beginning of data area.
18	Report Expanded Instruction Set	Pulses the BUSY- line if it supports the Expanded command set (commands 19, 28, and 29.)
19	Report Drive/Cartridge Type	Pulses the BUSY- line. The controller responds with "N" step pulses to inquire about a specific status condition.
20	Seek Track 0	Initiates tape motion and seeks track 0
21	Seek Track 1	Initiates tape motion and seeks track 1
22	Seek Track 2	Initiates tape motion and seeks track 2
23	Seek Track 3	Initiates tape motion and seeks track 3
24	Seek Track 4	Initiates tape motion and seeks track 4
25	Seek Track 5	Initiates tape motion and seeks track 5
26	Seek Track 6	Initiates tape motion and seeks track 6
27	Seek Track 7	Initiates tape motion and seeks track 7

(Continued)

Table 10-2. 40-MB Fixed Disk Drive Back-up Command Summary (Concluded)

Step Pulses	Command	Action
28	Seek Track "N"	Pulses BUSY- line. The controller responds with "N" step pulses.
29	Erase Tape	Erases entire tape.
31	Servo Write	Writes servo pattern on blank cartridge. The drive must be in Format mode.
32	Recalibrate	Sends simulated "at track 0" status to multipurpose controller board for diskette drive compatibility.

Command 19 causes the drive to pulse the BUSY- line. The controller responds with "N" pulses to inquire for a specific status condition. Table 10-3 gives the pulses used for the various status conditions.

Table 10.3. BUSY- Line Pulses for Status

"N" Step Pulses	Status Condition	Drive BUSY- Response	Status
4	Cartridge type	Low	DC2000 cartridge in drive.
		High	DC1000 cartridge in drive.
5	Servo density	Low	High-density, servo written, transfer rate at 500 kHz, R/W speed at 50 IPS.
		High	Low-density, servo written or blank cartridge. Transfer rate at 500 khz, R/W speed at 39 IPS.
6	Drive type	Low	40-MB drive
		High	10-MB drive

10.4 TAPE FORMATTING

The MS-DOS COMPAQ TAPE Utility Version 2 formats a tape by commanding the tape drive to perform a Servo Write process. The Servo Write process divides the tape into sections called servo blocks.

The TAPE Utility then writes formatting data into the servo blocks. Each of the 20 tape tracks is formatted by the 765 diskette controller to yield eighteen 1024-byte sectors per block. The data is written in double-density or modified frequency modulation (MFM) with the same layout as a standard diskette track. Table 10-4 gives the data format for the tape.

Table 10-4. Tape Data Format

	Nominal Value(hex)	Number of Bytes
(Index pulse) Pre-index Gap	4E	80
Pre-index Address Mark Sync	00	12
Index Address Mark	FC(Note 1)	4
Gap 1	4E	50
Pre-ID AM Sync	00 (Note 2)	12
ID Address Mark	FE (Note 3)	4
Sector ID	xx (Note 4)	4
Sector ID CRC	xx	2
Gap 2	4E	22
Pre-Data AM Sync	00	12
Data Address Mark	FB (Note 3)	4
Data	xx	1024
Data CRC	xx	2
Gap 3	4E	54
Gap 4	4E	(until second index pulse)

Notes:
1. First 3 bytes are C2 with missing clock transition between bits 3 and 4.
2. The boxed field is written once for each sector in the block with appropriate sector ID values for each sector written.
3. First 3 bytes are A1 with missing clock transition between bits 4 and 5.
4. xx = data dependent.

The Gap 3 value (54 bytes) shows the gap size when the tape is formatted. The Gap 3 size specified in the read/write commands is smaller (23 bytes). The size of Gap 4 depends on the tape speed. The 765 keeps writing until the second index pulse occurs.

The boxed field is written once for each sector in the block, with appropriate sector ID values for each sector written. The sector ID consists of four 1-byte fields that are used to identify each sector (using diskette mnemonics):

CYL	HEAD	SECT	SIZE	(CRC)	(CRC)

Cylinder = 0..123 Tape block number
Head = 0 (Not used)
Sector = 1..18 Sector number (within tape block)
Size = 3 Sector size (3 denotes 1024 bytes)

10.5 FILE STORAGE ON THE TAPE

The TAPE Utility places two types of descriptive information called the tape header (HDR) and the file allocation table (FAT) at the begining of the tape (Track 0, Block 0). The HDR is written to the tape first, followed by the FAT.

When a set of files is written to the tape, the HDR and the FAT are modified to reflect the new tape status. A Save Set Description is written to the beginning of each set of files (sequential backups). A redundant copy of the HDR and FAT is stored in Track 0, Block 1. If the first block becomes unreadable, the information in the second block is used to retrieve the data on the tape. All remaining blocks contain directory and file information.

The COMPAQ TAPE Utility generates an error correction code (ECC) that is stored in the last two sectors of each block, which is shown in Figure 10-3.

	Sector							
Block	1	2	3	...	15	16	17	18
0	HDR	FAT	FAT	...	FAT	FAT	ECC	ECC
1	HDR	FAT	FAT	...	FAT	FAT	ECC	ECC
2	FILES						ECC	ECC
.								
.								
.								

Figure 10-3. Tape Track 0 Data Format

The following sections describe the organization of data on a tape.

Tape Header

The tape header (HDR) occupies the first 1024-byte sector on the tape, which is shown in Figure 10-4. The tape header is divided into three parts: the Tape Identification (TID) area, the Save Set structures, and a reserved area.

1024 Bytes		
64 Bytes	768 Bytes	192 Bytes
TID	Save Set Description	Reserved

Figure 10-4. Tape Header

Tape Identification Area

Table 10-5 lists the contents of the Tape Identification area. Table 10-6 further explains the contents of the Tape Identification area.

Table 10-5. Tape Identification Area

Function	Bytes
Reserved (must be zero)	2
Volume name	32
Create (format) time	2
Create (format) date	2
Tracks per tape	2
Blocks per track	2
Sectors per block	2
Bytes per sector	2
Tape number	2
More flag (for multiple-tape back-up)	2
Backup time	2
Backup date	2
Program version (in BCD)	2
Format type	2
Reserved	6

Table 10-6. Tape Identification Area Parameters

Parameter Name	Description
Volume name	Up to 31 characters in length, padded with zeros to 32 bytes, resulting in a 'standard' null-terminated string.
Date/time the tape was initialized	Set only when the tape is formatted (by TAPE FORMAT), and is not updated by a normal TAPE BACKUP operation. (See Figure 10-6.)
Number of tracks per tape	20 for 40-MB tape, numbered 0..19
Number of intra-servo blocks per tape track	124 for 40-MB tape, numbered 0..123
Number of sectors per block	18 for 40-MB tape, numbered 1..17
Number of bytes per sector	1024
Tape number	The number of this tape in a multi-tape backup set. For a single-tape backup, this entry would be 1.
More flag	This word is set to 1 to indicate that there are additional tapes in the backup set, or 0 to indicate that this is the last tape in the set. For a single tape backup, this entry would be 0.
Date/time	The Date/time is written by TAPE BACKUP when the tape was backed-up and updated. (See Figure 10-5.)
TAPE Utility Version (in BCD)	The version of the COMPAQ TAPE Utility that wrote the tape.
Format Descriptor	The low byte of this word appears at offset +56 in the first sector of the tape. The format descriptor is used by the software to determine the tape format by recognizing the following codes: 0 - Tape is unused 1 - Reserved 2 - Reserved 3 - Tape used by COMPAQ TAPE Utility prior to Version 1.10 4 - Tape used by COMPAQ TAPE Utility Version 1.10 and later

Figure 10-5 shows the format of the time and date parameters of the Tape Identification area.

Bits

15..11	10..5	4..0
Hour (0–23)	Minute (0–59)	Seconds/2 (0–29)

Bits

15..9	8..5	4..0
Year–1980 (0–119)	Month (1–12)	Day (1–31)

Figure 10-5. Time and Date Format

Save Set Descriptions

The COMPAQ DOS Version 2 COMPAQ TAPE Utility supports multiple backups per tape. Each time a set of files is backed up to the tape, a Save Set description containing 24 bytes is written to the Tape Header. Up to 32 Save Set descriptions can be stored in the 768-byte Save Set description area of the Tape Header. Table 10-7 lists the 24-byte Save Set parameters.

Table 10-7. Save Set Description

Function	Bytes
Backup time	2
Backup date	2
Version	2
Save Set label	12
Start block	2
Source drive	1
Reserved byte	1
Reserved word	2

Table 10-8 further explains the contents of the Save Set description.

Table 10-8. Save Set Description Parameters

Parameter Name	Description
Backup time	Date/time the Save Set was backed up. This entry in the last non-blank Save Set matches the backup time and data located in the TID area.
Tape Utility Version (in BCD)	The version of the COMPAQ TAPE Utility that wrote the tape.
Starting block of Save Set	Tape block number where Save Set begins.
Backup source drive	Fixed disk or diskette drive from which the Save Set was backed up.
Save Set label	Save Set label, up to 11 characters in length. padded with zeros to 12 bytes, resulting in a standard null-terminated string.

File Allocation Table

The file allocation table (FAT) controls the assignment of sectors on the tape. For every sector on the tape, except for sectors containing ECC information, two bits are maintained in the FAT that describe the current state of that sector:

FAT Entry	Sector Status
0 0	Not allocated
0 1	Start of a file (header)
1 0	Allocated
1 1	Bad sector

Each FAT byte contains four 2-bit fields, with the least-significant bits describing the first sector. The FAT has allocation entries for the entire tape, including the tape HDR and FAT sectors. The entries for these sectors are "allocated".

Not all 15 available sectors are used for the FAT (not all are necessary). The size (in bytes) of the FAT for a tape can be determined by the following formula:

(Tracks x blocks per track x sectors per block)/4

For a 40-MB tape, the FAT table is:

(20 tracks x 124 blocks per track x 16 sectors per block)/4 = 39680/4 or 9920 bytes/FAT

Example: A 40-MB tape with no bad blocks contains two files, one which occupies 1 sector, and one which occupies 3 sectors. The first 10 bytes of the FAT would appear as follows:

FAT entries for first block on tape:

10101010	10101010	10101010	10101010
AA	AA	AA	AA

FAT entries for second block on tape:

10101010	10101010	10101010	10101010
AA	AA	AA	AA

FAT entries for files:

10100101	00000000
A5	00

Directory Information

All blocks after 0 and 1 on track 0 contain directory and file information. If the backup spanned multiple directories, the first sector(s) of the Save Set contain directory information. This information tells the COMPAQ TAPE Utility which directories to create on the destination disk during the Tape Restore process. These sectors are marked as allocated in the FAT.

Table 10-9 lists the format of the directory information.

Table 10-9. Directory Information

Function	Bytes
Directory name 1	78
Last entry flag	2
Reserved for future use	2
.	
.	
.	
Directory name x	78
Last entry flag	2
Reserved for future use	2

Table 10-10 lists the directory information parameters.

Table 10-10. Directory Information Parameters

Parameter Name	Description
Directory name	Directory pathname, padded with zeros to 78 bytes, resulting in a standard null-terminated string.
Last entry flag	This word has a value of 1. It marks the end of the directory name list.
Reserved	

Only the pathnames of the lowest level subdirectories are saved. All intermediate subdirectories can be recreated from these.

Example: The following directory names are generated for the directory shown in Figure 10-6:

```
\DOS
\TOOLS\EDITOR
\MISC\REPORTS\TEMP
\MISC\MEMOS
\MISC\EXPENSE
```

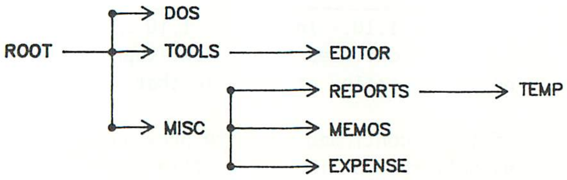


Figure 10-6. Sample Directory

File Information

Following the directory information (if any) are the sectors containing the file information.

The first sector of each file contains a header, which contains various information about the file.

Table 10-11 describes the file information. The tape file information parameters are described in Table 10-12.

Table 10-11. File Information

Function	Bytes
Header Signature (AAh,55h)	2
Filename	108
File Attribute	2
Original File Time	2
Original File Date	2
File Size (in bytes)	4
Backup Time	2
Backup Date	2
Aux File Attribute #1	2
Aux File Attribute #2	2

Table 10-12. Tape File Information Parameters

Parameter Name	Description
Header Signature	The 2-byte header signature is AAh, 55h. This signature is used to identify the header or separate it from the rest of the tape information.
Filename	The filename may be up to 107 characters in length, padded with zeros to 108 bytes, resulting in a standard null-terminated string. There is no structure imposed on the filename other than maximum length, but the COMPAQ TAPE Utility expects a DOS-style pathname (without a drive letter).
File Attribute	This word value is used by the COMPAQ Tape Utility to retain the original attributes of the file as specified by the operating system. For MS-DOS, only the low-order byte is used.
Original Date/time	Original date/time of the file. The format of the date and time values is shown in Figure 10-7.
File Size	32-bit file size (in bytes)
Backup Time and Date	The date and time the file was backed-up. This value is the same as the corresponding value in the headers of all the other files that were part of the same backup (see Figure 10-7).
Aux File Attribute #1	Not used in COMPAQ TAPE Utility prior to Version 1.10. In Version 1.10 and later: Bit 0, if set (=1), means that this file is continued on the next tape. In this case, the file size indicates only the portion of the file that is on this tape. Bit 1, if set (=1), means that this file is continued from the previous tape. In this case, the file size indicates only the portion of the file that is on this tape. If bit 1 is set (=1), with bit 0 reset (=0), this is the last portion of the file.
Aux File Attribute #2	Reserved, must be 0.

Figure 10-7 shows the format of the date and time information.

Bits

15..11	10..5	4..0
Hour (0–23)	Minute (0–59)	Seconds/2 (0–29)

Bits

15..9	8..5	4..0
Year–1980 (0–119)	Month (1–12)	Day (1–31)

Figure 10-7. Time/Date Format

Note: Any empty sectors in the last block of a Save Set are marked as allocated on the FAT.

10.6 CONNECTORS

The 40-MB Fixed Disk Drive Back-up uses the same cable, connectors, and pin arrangements as the diskette drives for the connections to the Multipurpose Fixed Disk Controller Board and the DC power supply.

The signal functions are different, however, and special software drivers are used to control the 40-MB Fixed Disk Drive Back-up. Table 10-13 shows the signal functions.

Table 10-13. Drive Logic Board to Drive Controller Signal Descriptions

Signal Name	Function
DRIVE 4 (TAPE) SELECT-	Drive select 4 is used to select 40-MB Fixed Disk Drive Back-up.
INDEX-	Indicates to the multipurpose fixed disk controller that one block has passed.
READ DATA-	This is the data stream of data and clock pulses from the 40-MB Fixed Disk Drive Back-up.
STEP-	Pulses give commands to the fixed disk drive back-up.
BUSY-	Indicates to the multipurpose fixed disk controller that the fixed disk drive back-up is still executing a command.
WRITE DATA-	This stream of data is written to the tape when WRITE GATE- is enabled.
WRITE GATE-	Enables the drive-logic disk-write circuits so data from the WRITE DATA- signal is written.
WRITE PROTECT-	Indicates to the multipurpose fixed disk controller that the cartridge in the drive is write-protected.

Figures 10-8 and 10-9 show the 40-MB Fixed Disk Drive Back-up connectors.

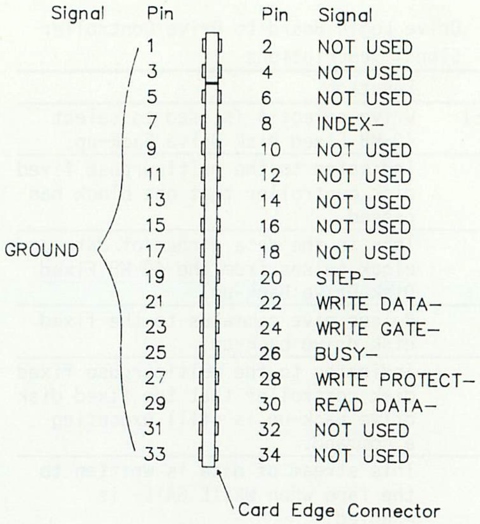
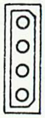


Figure 10-8. 40-MB Fixed Disk Drive Back-up Connector Pinout



Pin	**Signal**
1	+12 Vdc
2	Ground (+12 Vdc Return)
3	Ground (+5 Vdc Return)
4	+5 Vdc

Figure 10-9. 40-MB Fixed Disk Drive Back-up Power Connector Pinout

Chapter 11
VIDEO DISPLAY CONTROLLER SYSTEMS

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Chapter 11
VIDEO DISPLAY CONTROLLER

11.1 INTRODUCTION

Two COMPAQ video controllers are optionally available with COMPAQ DESKPRO 386: the COMPAQ Video Display Controller Board and the COMPAQ Enhanced Color Graphics Board. Information about the COMPAQ Enhanced Color Graphics Board is provided in a separate technical reference guide.

The COMPAQ video display controller board is described in this chapter. This board is compatible with color graphics adapters (CGA) and also provides several enhanced features. The most noticeable feature is the 9 x 14 high-resolution text that has been traditional on all other COMPAQ products. The high-resolution text is provided when the COMPAQ Dual-Mode Monitor is used with the COMPAQ Video Display Controller Board.

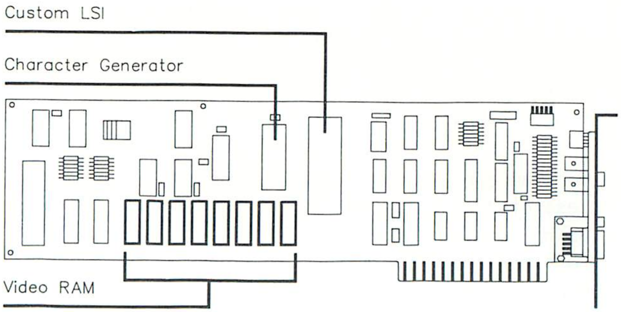


Figure 11-1. Video Display Controller Board

The video display controller board has the following features:

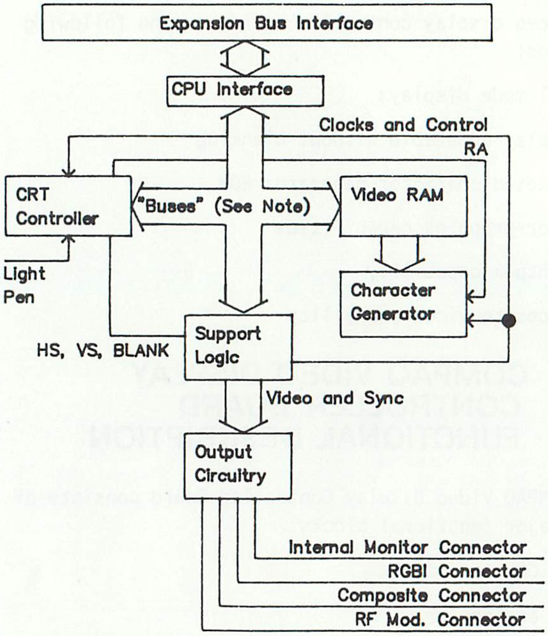
- Dual-mode displays
- Display updatable without blanking
- Socketed character-generator ROM
- Color-graphics capabilities
- Lightpen capability
- Composite-video capability

11.2 COMPAQ VIDEO DISPLAY CONTROLLER BOARD FUNCTIONAL DESCRIPTION

The COMPAQ Video Display Controller Board consists of five major functional blocks:

- The CPU interface
- CRT controller
- Support logic
- Video memory
- Character generator
- Output circuitry

Figure 11-2 shows the functional block diagram of the video display controller board.



Note: "Buses" includes the address, data, control, and decode buses.

Figure 11-2. Video Display Controller Board Functional Block Diagram

The following sections briefly describe each functional block.

CPU Interface

The CPU interface consists of address decoding logic, address bus buffers, and data bus transceivers. The video display controller uses the 8-bit bus to interface to the CPU. It does not require the full 16-bit bus expansion slot.

Address lines, together with the bus control signals, are used to decode valid I/O devices. The output lines of the decoders select the 6845, video memory, and other functions. The decoders also provide control of the data bus transceiver.

The interface circuitry allows shared access of video memory between the CPU and the 6845 by multiplexing address lines to the video memory. The CPU can access the video memory at any time without interfering with the display.

The interface circuitry also provides buffering for the reset signal and the 14.318-MHz clock.

Option jumpers J7 and J8 select a base I/O port address of 3DXh (standard) or a base I/O port address of 3BXh. Option jumper J9 selects a base memory address for the video memory of B8000h (standard) or B0000h.

CRT Controller

The CRT controller (6845) is an LSI device that generates the addresses and other signals that refresh the video memory. It also supplies the synchronization and blanking signals for the output circuitry.

The 6845 device contains 19 internal registers, all of which are I/O-mapped. The system BIOS programs the internal registers that control the display timing.

The 6845's lightpen register allows lightpen interactions for systems with monitors that are optically compatible (the COMPAQ Dual-Mode Monitor is not compatible due to medium-persistence phosphor).

Support Logic

The support logic consists primarily of a custom large scale intergration (LSI) circuit that provides several video functions.

- Converts data bytes from the video memory or the character generator into the individual dots on the display (shift register or serialization).
- Controls the application of the associated video attributes and conditions. The mode and color registers, and part of the status register are part of this device.
- Generates the memory timing and other clock signals for the 6845.

The support logic selects the high- or low-scan mode according to the character-height parameter written to the 6845's internal register 09h. A value of 0Dh in register 09h selects the high-scan mode.

Video Memory

The video memory on the video display controller consists of 16KB of static RAM beginning at address B8000h and extending to BBFFFh (Figure 11-3). The video memory is dual-ported so that the CPU can access it at any time without causing visual anomalies on the CRT display.

One wait state is automatically inserted on all video memory cycles by asserting the I/O READY- line on the expansion bus. The wait state is required for synchronization purposes.

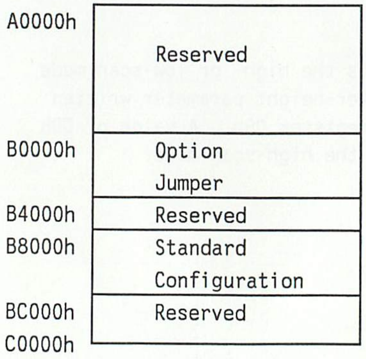


Figure 11-3. Video Memory Address Space

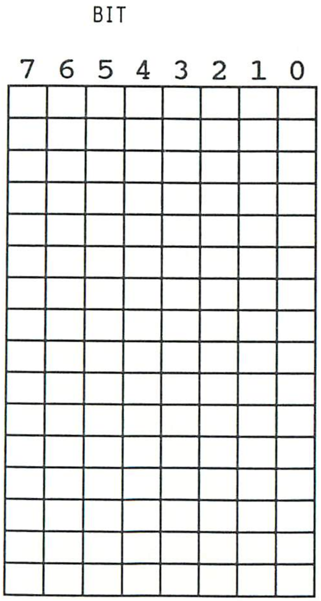
Character Generator

The character-generator ROM is an 8K x 8 static ROM. Special character sets can be supported by replacing the standard ROM (socketed) with a 250-ns, 2764-type EPROM. The CPU cannot read the ROM's contents--it is accessed only by the 6845, together with video RAM.

The 8K x 8 character generator ROM contains three character sets of 256 characters each. The first set is used for the 9 x 14 dot cell character set and takes up 4KB. From each group of 16 bytes, 14 are used to form the cell, with bytes +00h through +05h for the lower six displayed lines, and bytes +08h through +0Fh for the top eight scan lines. Scan line 0 is adjacent on the screen to scan line 13 of the character above.

The video display controller generates a ninth horizontal dot from an 8-bit-wide ROM for 9 x 14 dot cells. It replicates bit 0 (the eight dot) for graphics characters C0h through DFh. It places a blank dot in the ninth position for other characters. This scheme allows continuous horizontal lines and solid figures needed by certain graphics symbols.

The layout of the 9 x 14 dot cell is as follows:

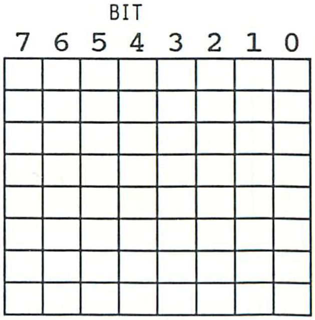


Offset	Scan line
+08h	0
+09h	1
+0Ah	2
+0Bh	3
+0Ch	4
+0Dh	5
+0Eh	6
+0Fh	7
+00h	8
+01h	9
+02h	10
+03h	11
+04h	12
+05h	13
+06h	(Not used)
+07h	(Not used)

The second and third sets are interleaved and occupy the remaining 4 KB. They provide standard and alternate 8 x 8 dot versions (selectable by jumper J1) of an 8 x 8 dot cell character font used by both 40- and 80-column low-scan text modes. Scan line 0 is adjacent on the screen to scan line 7 of the character above.

Note: A separate character font contained in the system ROM duplicates the first 128 standard 8 x 8 dot cells and is used by ROM BIOS routines to display text in one of the graphics display modes.

The second and third character sets in the VDU ROM have 8 x 8 dot cells and are interleaved every eight bytes. That is, the standard set begins at offset 1000h, and the alternate set begins at 1008h. The layouts are as follows:



Standard Set Offset	Alternate Set Offset
+00h	+08h
+01h	+09h
+02h	+0Ah
+03h	+0Bh
+04h	+0Ch
+05h	+0Dh
+06h	+0Eh
+07h	+0Fh

Example: Question mark (ASCII 3Fh) in the 9 x 14 dot cell.

Value	7	6	5	4	3	2	1	0	Address	Scan Line
00h									03F8h	0
00h									03F9h	1
3Eh			■	■	■	■	■		03FAh	2
63h		■	■				■	■	03FBh	3
63h		■	■				■	■	03FCh	4
06h						■	■		03FDh	5
0Ch					■	■			03FEh	6
18h				■	■				03FFh	7
18h				■	■				03F0h	8
00h									03F1h	9
18h				■	■				03F2h	10
18h				■	■				03F3h	11
00h									03F4h	12
00h									03F5h	13
00h									03F6h	(Not used)
00h									03F7h	(Not used)

Note: The bytes at addresses 03FBh and 03FCh have the least-significant bit = 1, but this bit is not right-extended into the 9th column because '?' lies outside of the special range C0h through DFh.

Example: Question mark (ASCII 3Fh) in the standard 8 x 8 dot cell.

Value	7	6	5	4	3	2	1	0	Address	Scan Line
78h		■	■	■	■				13F0h	0
CCh	■	■			■	■			13F1h	1
0Ch					■	■			13F2h	2
18h				■	■				13F3h	3
30h			■	■					13F4h	4
00h									13F5h	5
30h			■	■					13F6h	6
00h									13F7h	7

Example: Question mark (ASCII 3Fh) in the alternate 8 x 8 dot cell.

Value	7	6	5	4	3	2	1	0	Address	Scan Line
3Ch			■	■	■	■			13F8h	0
42h		■					■		13F9h	1
02h							■		13FAh	2
04h						■			13FBh	3
08h					■				13FCh	4
00h									13FDh	5
08h					■				13FEh	6
00h									13FFh	7

Output Circuitry

The output circuitry contains the logic and buffers required to interface the video display controller with a video display. The output circuitry can directly drive a composite video monitor, an RGBI TTL input monitor or a television, using an external RF modulator (not supplied).

The RGBI, composite, and RF modulator outputs are normally only active in the low-scan mode. The internal monitor interface is always enabled. The internal monitor interface is used with COMPAQ's portable products. When a COMPAQ Dual-Mode Monitor is used with the COMPAQ DESKPRO 386, jumper J3 and J5 are set to enable all video outputs for both modes.

11.3 PROGRAMMING THE VIDEO DISPLAY CONTROLLER

The video display controller is an I/O-mapped and memory-mapped (video memory) board. Table 11-1 lists the I/O addresses.

Table 11-1. Video Display Controller I/O Addresses

I/O Addr.	Read or Write	Register Description
3D4h	W	6845 Index
3D5h	R/W	6845 Data
3D8h	W	Mode
3D9h	W	Color
3DAh	R	Status
3DBh	W	Reset Lightpen
3DCh	W	Set Lightpen

Note: See Chapter 4 for general considerations for programming I/O devices.

6845 INDEX AND DATA REGISTERS (3D4h AND 3D5h)

The 6845 CRT controller is addressed as two port addresses. One port (3D4h) accesses the Index register. The other port (3D5h) accesses the Data register.

The CRT controller has 19 internal registers. The Index register counts as one of these, although it serves as a pointer to the other registers.

To write to or read from a 6845 register:

1. Load the 6845's register number into the Index register (3D4h).
2. Write or read the byte to/from the Data register (3D5h).

The registers pointed to with Index register values of 00h to 0Bh directly control the timing of the CRT controller and the associated waveform profiles which drive the display monitors. Before changing any of the default parameters in these registers, be sure that the environment is understood (that is, which monitors are connected to the video display controller and the timing that each display requires) for proper operation.

The initial register values are listed in Table 11-2.

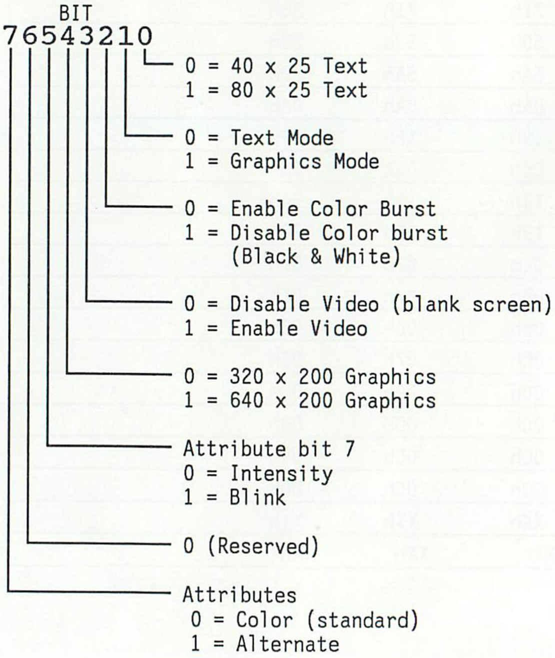
Table 11-2. Initial Values for 6845 Internal Registers

Index Reg.	Register Description	Read or Write	Recommended Values (Note 1)(Default) 40 x 25 Low-Scan	80 x 25 High-Scan	80 x 25 Low-Scan	Graphics Low-Scan
00h	Horizontal Total (characters)(Note 2)	W	38h	71h	71h	38h
01h	Horizontal Displayed (characters)	W	28h	50h	50h	28h
02h	Horizontal Sync Position (characters)	W	2Dh	5Ah	5Ah	2Dh
03h	Horizontal Sync Width (characters)	W	0Ah	0Ah	0Ah	0Ah
04h	Vertical Total (rows)(Note 3)	W	1Fh	19h	1Fh	7Fh
05h	Vertical Total Adjust (lines)(Note 4)	W	06h	06h	06h	06h
06h	Vertical Displayed (rows)	W	19h	19h	19h	64h
07h	Vertical Sync Position (rows)	W	1Ch	19h	1Ch	70h
08h	Interlace Mode & Skew	W	02h	02h	02h	02h
09h	Character Height (lines)	W	07h	0Dh	07h	01h
0Ah	Cursor Start (line)	W	06h	0Bh	06h	06h
0Bh	Cursor End (line)	W	07h	0Ch	07h	07h
0Ch	Display Start Address (high)	R/W	00h	00h	00h	00h
0Dh	Display Start Address (low)	R/W	00h	00h	00h	00h
0Eh	Cursor Address (high)	R/W	00h	00h	00h	00h
0Fh	Cursor Address (low)	R/W	00h	00h	00h	00h
10h	Lightpen Address (high)	R	XXh (Note 5)	XXh	XXh	XXh
11h	Lightpen Address (low)	R	XXh	XXh	XXh	XXh

Notes:
1. Recommended values apply to COMPAQ monitors.
2. Characters means character count.
3. Rows = vertical character units = 8 or 14 lines.
4. Lines = horizontal scan line elements that make up a character row.
5. X = undefined.

MODE REGISTER (3D8h, WRITE ONLY)

This register selects the current video-display mode in conjunction with other 6845 registers.



Bit 0. If bit 0 = 0, text is displayed in a 40-column mode. In the 40-column mode, the clock for the video and timing logic is divided by two.

If bit 0 = 1, text is displayed in an 80-column mode.

Bit 1. If bit 1 = 0 , the text mode is selected.

If bit 1 = 1, the bit-mapped graphics mode is selected.

Bit 2. If bit 2 = 0, color encoding on the composite video output is enabled. This bit only affects the composite video outputs; the other video outputs are unaffected.

If bit 2 = 1, the reference color burst signal for the composite video output is disabled (Black & White display).

Bit 3. If bit 3 = 0, the entire display is blanked, but the sync signals are still active.

If bit 3 = 1, the screen is displayed normally.

Bit 4. If bit 4 = 0, the display format is 320 x 200 in the graphics modes.

If bit 4 = 1, the display format is 640 x 200 in the graphics modes (Mode register bit 1 = 1).

The 640 x 200 mode is a 1 bit-per-pixel format, while the 320 x 200 mode is 2 bits per pixel.

Bit 5. This bit has meaning in the text modes only.

If bit 5 = 0, then bit 7 of the text-attribute byte controls the background intensity function.

If bit 5 = 1, then bit 7 of the text-attribute byte controls the blinking function.

Bit 6. Reserved (always 0)

Bit 7. This bit has meaning in the text modes only.

If bit 7 = 0 (standard), the text is displayed with the color attributes (color foreground and background). See the section entitled "Video Display Modes."

If bit 7 = 1, the text is displayed with the alternate attributes that define a white or black foreground or background and text underlining capability. This mode is only available when in the high-scan mode. The low-scan mode uses the color attributes regardless of the state of this bit.

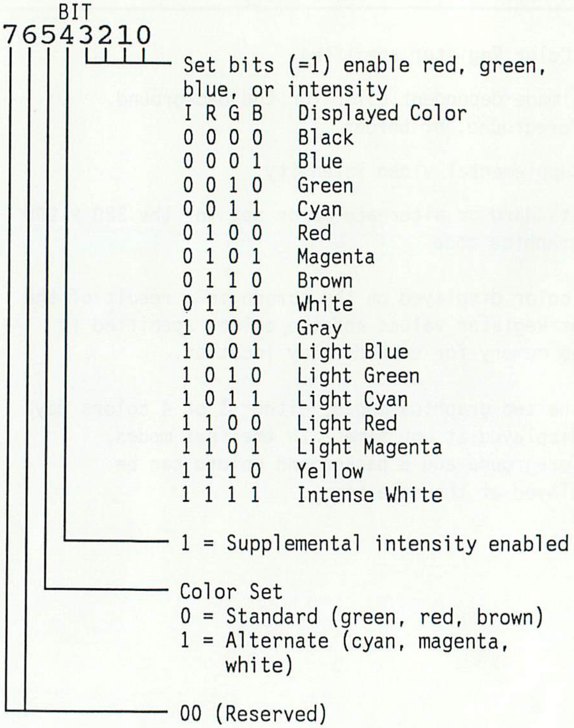
COLOR REGISTER (3D9h, WRITE ONLY)

The Color Register specifies:

- A mode-dependent color for the background, foreground, or border
- Supplemental video intensity
- Standard or alternate color set for the 320 x 200 graphics mode

The color displayed on the screen is a result of the Color Register values and the colors specified in video memory for each display location.

In the two graphics modes, either 1 or 4 colors may be displayed at one time. In the text modes, 16 foreground and 8 background colors can be displayed at the same time.



Set bits (=1) enable red, green, blue, or intensity

I	R	G	B	Displayed Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	Intense White

1 = Supplemental intensity enabled

Color Set
0 = Standard (green, red, brown)
1 = Alternate (cyan, magenta, white)

00 (Reserved)

Bits 3..0. These four bits select a mode-dependent color.

In the 640 x 200 graphics mode, they select the color of an active pixel.

In the 320 x 200 graphics mode, they select the color of an inactive pixel, or background.

In the 40 x 25 text mode, they select the color of the overscanned border.

Bit 4. If bit 4 = 0, unintensified colors are selected for both the 320 x 200 graphics mode and the background colors in the text mode.

If bit 4 = 1, intensified colors are selected for both the 320 x 200 graphics mode, and background colors in the text mode.

Bit 5. Selects the color set used in the 320 x 200 graphics mode.

If bit 5 = 0, the standard color set is selected. The standard set consists of green, red, and brown.

If bit 5 = 1, the alternate color set is selected. The alternate set consists of cyan, magenta, and white.

Bits 7..6. Bits 7 and 6 are always 0 (reserved).

STATUS REGISTER (3DAh, READ ONLY)

The Status Register contains real-time event status information.

```
    BIT
76543210
||||||||
|||||||└─ 0 = Active Display
|||||||   1 = Retrace Interval
||||||└─── 0 = Lightpen Latch not triggered
||||||     1 = Lightpen Latch triggered
|||||└──── Lightpen Switch State
||||└───── 1 = Vertical Retrace in progress
└┴┴┴────── 0000 (Not used)
```

Bit 0. If bit 0 = 0, the video raster is on the active (displayed) area of the screen.

If bit 0 = 1, the video raster is in a horizontal or vertical retrace period.

Bit 1. This bit reflects the state of the lightpen latch.

If bit 1 = 1, the lightpen has triggered--the 6845 lightpen address registers may contain a valid address. The state of the lightpen latch can be cleared by writing to port 3DBh and set by writing to 3DCh.

Bit 2. This bit reflects the state of the lightpen switch signal of the lightpen interface connector. This signal is not latched or debounced.

Bit 3. This bit reflects the state of the vertical sync signal.

If bit 3 = 1, the vertical retrace signal is active.

CLEAR OR SET LIGHTPEN LATCH (3DBh and 3DCh, WRITE ONLY)

By writing any value to port 3DBh, the lightpen latch bit of the status register will be reset to 0.

By writing any value to port 3DCh, the lightpen latch bit of the status register will be set to 1.

Bit 1 of the status register (3DAh) defines the lightpen latch status.

11.4 VIDEO DISPLAY MODES

The video display controller displays either graphics or text.

Text displays are character-oriented. The dot patterns for the display is stored in a character-generator ROM. Text on COMPAQ monitors is normally displayed in the high-scan mode. (See "Monitors Supported," in this chapter.)

Graphics displays are pixel-oriented. The color of each pixel is specified in video memory. A pixel is the smallest controllable display element--a single dot on the screen. Graphics on COMPAQ monitors are displayed in the low-scan mode.

Figure 11-4 compares the pixel patterns for the 9 x 14 and 8 x 8 pixel text characters.

```
---------
---------
----■----                         --■■----
---■■■---                         -■■■■---
--■■-■■--                         ■■--■■--
-■■---■■-                         ■■--■■--
-■■■■■■■-                         ■■■■■■--
-■■---■■-                         ■■--■■--
-■■---■■-                         ■■==■■==  Cursor line
-■■---■■-                         ========  Cursor line
=========  Cursor line
=========  Cursor line
---------

9 x 14 Character Format      8 x 8 Character Format
```

Figure 11-4. Comparison of Text Character Formats

Text Displays

For text displays, the video display controller uses 2 bytes of video memory to define each character: the character byte and the attribute byte.

The character byte (even address) is sent to the character generator. The character generator provides the patterns for that character code.

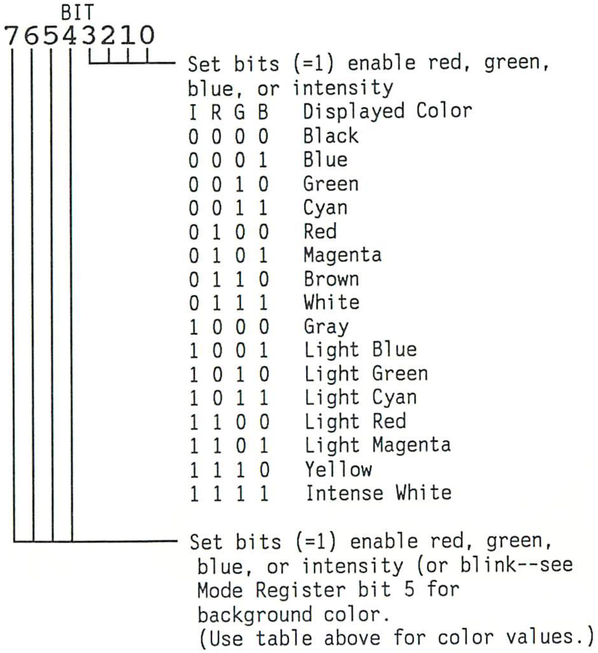
The attribute byte (odd address) specifies the foreground and background color to use for the character and whether the character should be intensified or blinking (see the Mode Register described previously).

Table 11-3 lists the character codes and the resulting characters defined in the character generator. The table displays the characters in a hexadecimal format. For example, 20h is the value for the space character.

Table 11-3. Character Codes

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		☺	☻	♥	♦	♣	♠	•	◘	○	◙	♂	♀	♪	♫	☼
1	►	◄	↕	‼	¶	§	▬	↨	↑	↓	→	←	∟	↔	▲	▼
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	¦	}	~	⌂
8	Ç	ü	é	â	ä	à	å	ç	ê	ë	è	ï	î	ì	Ä	Å
9	É	æ	Æ	ô	ö	ò	û	ù	ÿ	Ö	Ü	¢	£	¥	₧	ƒ
A	á	í	ó	ú	ñ	Ñ	ª	º	¿	⌐	¬	½	¼	¡	«	»
B	░	▒	▓	│	┤	╡	╢	╖	╕	╣	║	╗	╝	╜	╛	┐
C	└	┴	┬	├	─	┼	╞	╟	╚	╔	╩	╦	╠	═	╬	╧
D	╨	╤	╥	╙	╘	╒	╓	╫	╪	┘	┌	█	▄	▌	▐	▀
E	α	β	Γ	π	Σ	σ	µ	τ	Φ	Θ	Ω	δ	∞	φ	ε	∩
F	≡	±	≥	≤	⌠	⌡	÷	≈	°	∙	·	√	ⁿ	²	■	

Figure 11-5 shows the text attribute byte values (with Mode Register bit 7 = 0).



Set bits (=1) enable red, green, blue, or intensity

I	R	G	B	Displayed Color
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	White
1	0	0	0	Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	Intense White

Set bits (=1) enable red, green, blue, or intensity (or blink--see Mode Register bit 5 for background color. (Use table above for color values.)

Figure 11-5. Attribute Byte for Color Text

Figure 11-6 shows the alternate text-attribute byte values (with Mode Register bit 7 = 1)

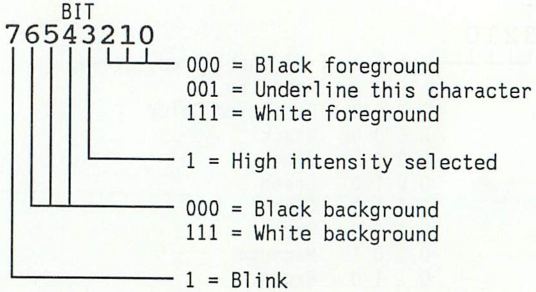
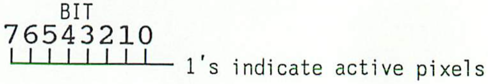


Figure 11-6. Alternate Attribute Byte (80 x 25, High-Scan Text Only)

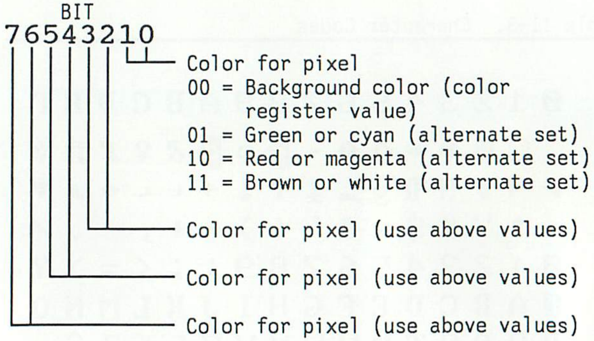
Graphics Displays

For pixel-oriented displays, the video display controller uses video memory as the source of the patterns to display.

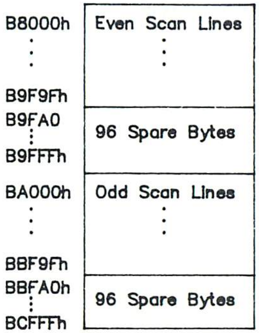
In the 640 x 200-pixel graphics mode, a single byte of video memory defines the state of eight pixels. Bit 7 is the left-most pixel on the display. The color used for active pixels is specified in the color register.



In the 320 x 200-pixel graphics mode, a single byte defines the state of four pixels (two bits per pixel). The two bits that define a pixel specify one of three colors from the standard or alternate color set or the background color. Bits 7 and 6 control the leftmost pixel.


BIT
76543210
Color for pixel
00 = Background color (color register value)
01 = Green or cyan (alternate set)
10 = Red or magenta (alternate set)
11 = Brown or white (alternate set)
Color for pixel (use above values)
Color for pixel (use above values)
Color for pixel (use above values)

For the graphics modes, the video memory is divided into separate blocks for the even and odd scan lines. Figure 11-7 shows the format of video memory for the graphic modes.



Addresses for Graphics

Row	First Column	Last Column (First Column plus 80)
1	B8000h	B804Fh
2	BA000h	BA04Fh
3	B8050h	B809Fh
4	BA050h	BA09Fh
⋮	⋮	⋮
197	B9F00h	B9F4Fh
198	BBF00h	BBF4Fh
199	B9F50h	B9F9Fh
200	BBF50h	BBF9Fh

Figure 11-7. Format of Video Memory for the Graphic Modes

11.5 MONITORS SUPPORTED

The video display controller supports the following types of monitors:

- COMPAQ Dual-Mode Monitor
- COMPAQ Color Monitor or other red-green-blue-intensity (RGBI) color monitors that connect to the standard DB-9 (9-pin) connector
- Monochrome or color monitors that require composite-video signals may use an RCA-type connector or a recessed Berg connector.

Dual-Mode Monitor

The COMPAQ Dual-Mode Monitor supports two different display modes, with different scanning frequencies for each mode. The high-scan mode is used by the COMPAQ Video Display Controller Board to generate high-resolution text while providing compatibility with software products developed for color graphics adapters (CGA).

The high-scan mode has a horizontal scan frequency of 18.5 kHz and a vertical scan frequency of 50 Hz, non-interlaced. High scan supports the text modes, using a 9 x 14-pixel character block. This mode has 350 active vertical lines for 25 rows of 14-pixel-high characters, and 720 horizontal pixels for 80 columns of 9-pixel-wide characters.

Chapter 12 provides a detailed description of the COMPAQ Dual-Mode Monitor.

COMPAQ Color Monitor or Other RGBI Monitors

RGBI monitors receive their video signals in the form of separate lines for the red, green, and blue colors, intensity, horizontal sync, and vertical sync. These are all TTL-level signals. With four signals (red, green, blue, and intensity) to specify color, 16 colors or shades of gray are available. Monitors that do not support the intensity signal are limited to eight colors.

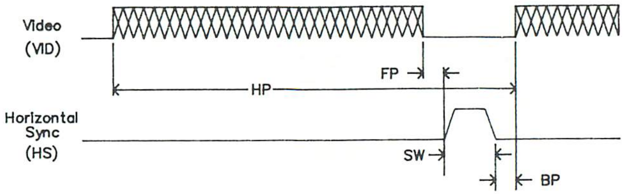
The COMPAQ Video Display Controller Board does not support high-resolution (9 x 14) text with the COMPAQ Color Monitor or other RGBI monitors. Chapter 12 provides a detailed description of the COMPAQ Color Monitor.

Composite Video Monitors

Composite video monitors, or other video equipment with composite video inputs, connect to the RCA-type jack provided on the mounting bracket. If a monochrome display is used, disable the color burst signal to reduce interference.

An external RF modulator can be connected to either the RCA-type connector or the recessed Berg connector for use with television receivers. The Berg connector provides the same video signal as the RCA-type connector plus a +12 V power connection. Due to television bandwidth limitations, 80-column television displays are not recommended.

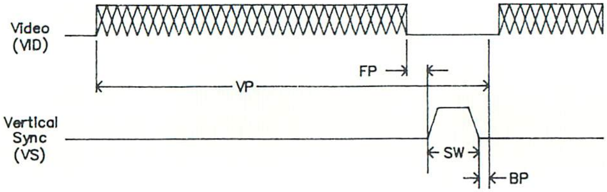
Figure 11-8 shows the timing characteristics for the horizontal sync signals.



Symbol	Parameter	High Scan	Low Scan
HP	Horizontal Period	54.1 μs	63.7 μs
FP	Front Porch	5.7 μs	6.7 μs
SW	Sync Width	3.8 μs	4.5 μs
BP	Back Porch	6.6 μs	7.8 μs

Figure 11-8. Horizontal Timing

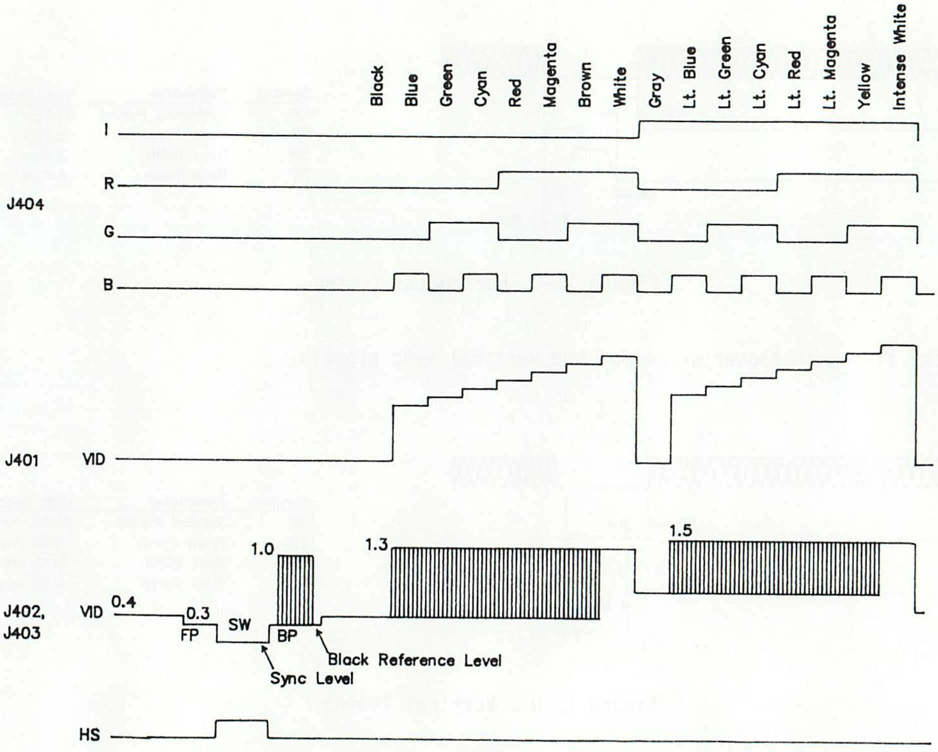
Figure 11-9 shows the timing characteristics for the vertical sync signals.



Symbol	Parameter	High Scan	Low Scan
VP	Vertical Period	20.00 ms	16.68 ms
FP	Front Porch	0.00 ms	1.53 ms
SW	Sync Width	0.16 ms	0.19 ms
BP	Back Porch	0.92 ms	2.23 ms

Figure 11-9. Vertical Timing

Figure 11-10 shows the characteristics for the video connectors.



Notes: 1. Burst is only present in the 40 x 25 text mode or the 320 x 200 graphics mode.
2. This is a block-frame format without equalization pulses.

Figure 11-10. Video Display Controller Output Signal Waveforms

11.6 JUMPERS

Jumpers J1 through J9 change the configuration of the video display controller board. Only J3 and J5 have pins and shorting blocks installed. Other jumpers are etched on the board.

Table 11-4 lists the jumpers for the video display controller board. Figure 11-11 shows the video display controller board jumpers.

CAUTION
Modifying etched jumpers invalidates the COMPAQ warranty of the board.

Table 11-4. Jumpers on the Video Display Controller Board

J1 - 8 x 8 Character Set Jumper

The character generator ROM contains two complete sets of 8 x 8 dot lookup tables. The standard table is suitable for all types of monitors. The alternate table provides sharper character set for 40-column displays on televisions. This jumper is etched on the board.

J1	Configuration
2-3	Standard 8 x 8 cell
1-2	Alternate 8 x 8 cell

(Continued)

Table 11-4. Jumpers on the Video Display Controller Board (Continued)

J2 - Vertical Sync Polarity

The vertical sync signals can have positive (standard) or negative polarity. This jumper is etched on the board.

J2	Configuration
1-2	Positive vertical sync (standard)
2-3	Negative vertical sync

J4 - Horizontal Sync Polarity

The horizontal sync signals can have positive (standard) or negative polarity. This jumper is etched on the board.

J4	Configuration
2-3	Positive horizontal sync (standard)
1-2	Negative horizontal sync

J3, J5 - External High-Scan Video

These jumpers control all but the internal monitor. Video outputs will be active in high scan. They are changed as a set (both to 2-3 or both to 1-2).

J3	J5	Configuration
2-3	2-3	Enable high-scan video on external outputs (standard setting for COMPAQ DESKPRO 386)
1-2	1-2	Disable high-scan video on external outputs (standard setting for COMPAQ portable computers)

(Continued)

Table 11-4. Jumpers on the Video Display Controller Board (Concluded)

J6 - Enable Mode Signal
This 2-pin jumper is always set for 1-2.

J7, J8, and J9 are reserved.

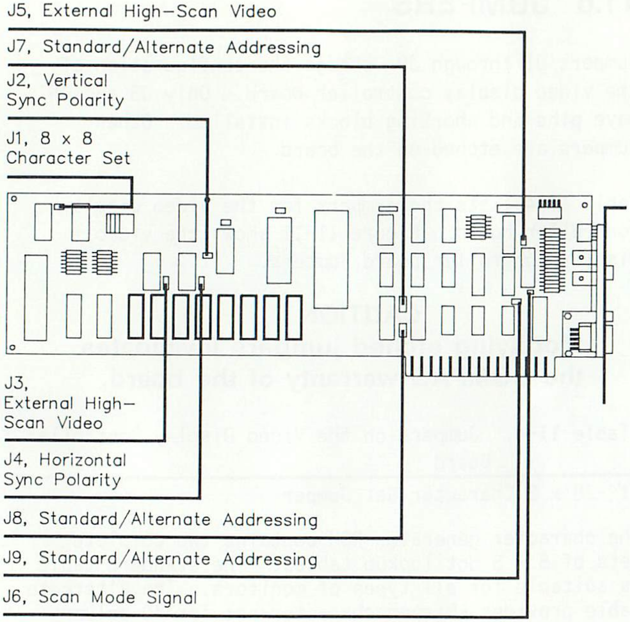

J5, External High–Scan Video
J7, Standard/Alternate Addressing
J2, Vertical Sync Polarity
J1, 8 x 8 Character Set
J3, External High–Scan Video
J4, Horizontal Sync Polarity
J8, Standard/Alternate Addressing
J9, Standard/Alternate Addressing
J6, Scan Mode Signal

Figure 11-11. Video Display Controller Jumpers

11.7 CONNECTORS

Figure 11-12 through 11-17 show the video display controller board connectors.

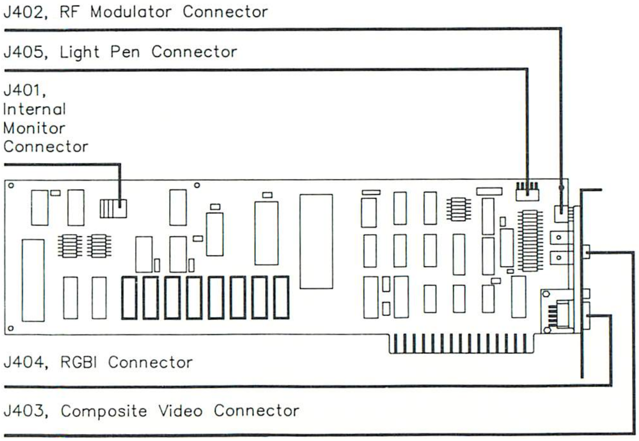

J402, RF Modulator Connector
J405, Light Pen Connector
J401, Internal Monitor Connector
J404, RGBI Connector
J403, Composite Video Connector

Figure 11-12. Video Display Controller Connectors

Table 11-5. J401, Internal Monitor Connector Signals

Signal	Pin	I/O	Description
Chassis Ground	11,12	-	Cable Shield
HS	7	0	Horizontal sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is always fixed at 8 characters regardless of the duration programmed in the 6845. See the section entitled "Monitors Supported" for the timing characteristics.
MODE	3	0	This TTL signal controls the monitor mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The MODE signal is high (= 1) for the low-scan mode, and low (= 0) for the high-scan mode.
Signal Ground	2,4,8	-	This is the ground reference for the TTL signals.
VID	5	0	This analog video output signal ranges from 1.0 VDC (black) to 2.5 VDC (white) into 470 to 6800 ohms (impedance). Its ground reference is the video ground signal (pin 6).
Video Ground	6	-	This is the ground reference for the VID signal (pin 5).

(Continued)

Table 11-5. J401, Internal Monitor Connector Signals (Concluded)

Signal	Pin	I/O	Description
VS-	1	0	Vertical sync is an active-low TTL signal in both level and drive characteristics. The pulse duration is always fixed to three scan lines regardless of the duration that is programmed in the 6845's internal registers. Refer to the section entitled "Monitors Supported" for the timing characteristics for the vertical sync signals.

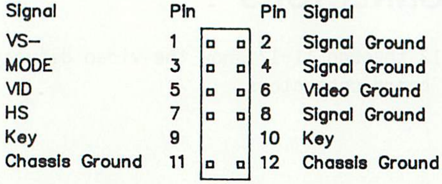


Figure 11-13. J401, Internal Monitor Connector

Table 11-6. J402, RF Modulator Connector Signals

Signal	Pin	I/O	Description
+12 VDC	1	0	Power
COMPOSITE VIDEO	3	0	This analog signal is the composite video output.
Signal Ground	4	-	Reference for composite video

Table 11-7. J403, Composite Video Connector Signals

Signal	Pin	I/O	Description
Chassis Ground	2	-	Reference for composite video
COMPOSITE VIDEO	1	0	This analog signal is the composite video output.

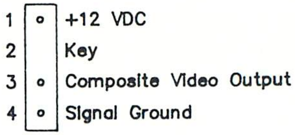


Figure 11-14. J402, RF Modulator Connector

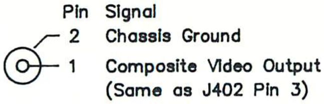


Figure 11-15. J403, Composite Video Connector

Table 11-8. J404, RGBI Video Connector Signals

Signal	Pin	I/O	Description
B	5	O	Blue. Active-high TTL signal.
G	4	O	Green. Active-high TTL signal.
HS	8	O	Horizontal sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is fixed at eight characters regardless of the duration programmed in the 6845. Refer to the entitled "monitors Supported" for the timing characteristics.
I	6	O	Intensity. Active-high TTL signal.
MODE	7	O	This signal controls the monitor high- or low-scan mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The MODE signal is high for the low-scan mode and low for the high-scan mode.
R	3	O	Red. Active-high TTL signal.
Signal Ground	1,2	-	TTL signal reference
VS	9	O	Vertical sync is an active-high TTL signal in both level and drive characteristics. The pulse duration is fixed to 3 scan lines regardless of the pulse duration programmed in the 6845. Refer to the section entitled "Monitors Supported" for the timing characteristics.

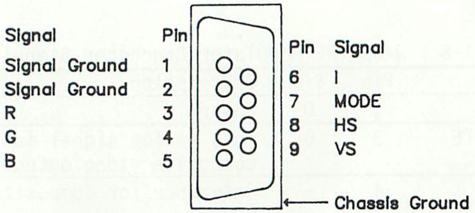


Figure 11-16. J404, RGBI Connector

Table 11-9. J405, Lightpen Connector Signals

Signal	Pin	I/O	Description
+5 VDC	5	O	+5 VDC lightpen power source
+12 VDC	6	O	+12 VDC lightpen power source
LIGHTPEN SWITCH-	3	I	Active-low signal indicates lightpen switch contact closed
LIGHTPEN TRIGGER-	1	I	Active-low signal indicates lightpen triggered
Signal Ground	4	-	Reference for TTL signals

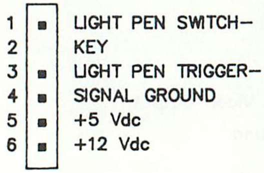
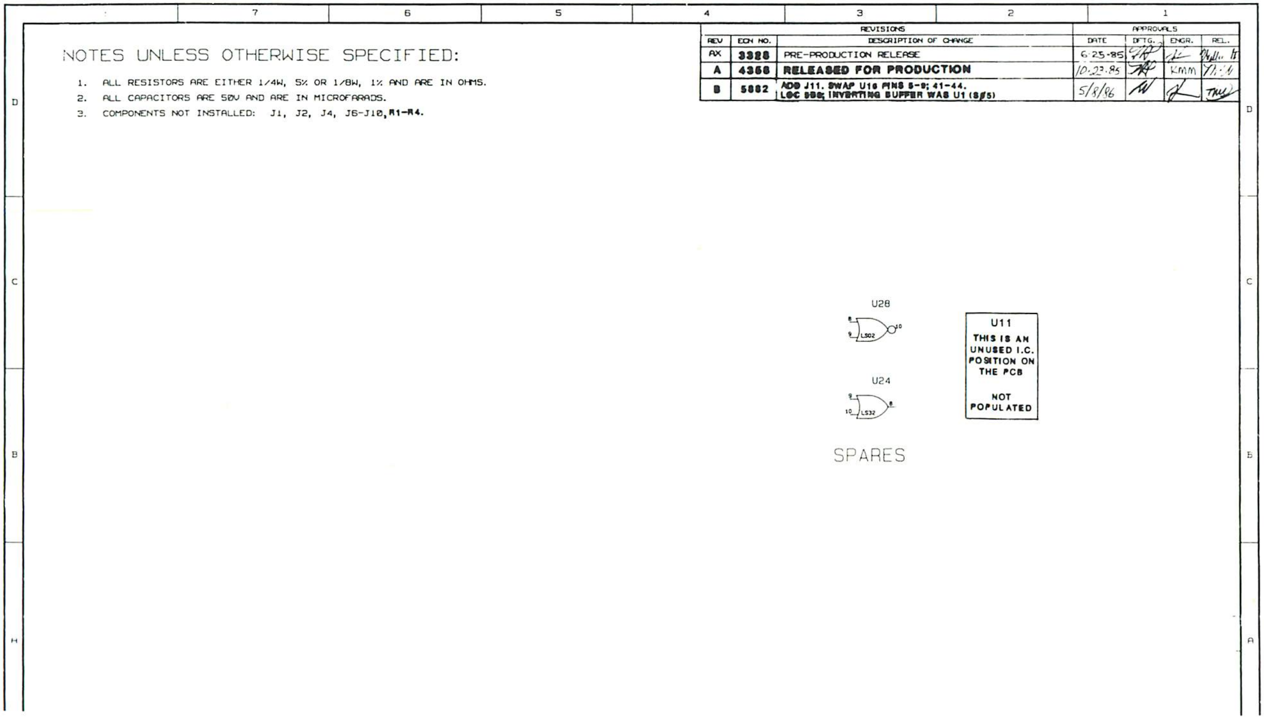


Figure 11-17. J405, Lightpen Connector

11.8 SCHEMATICS

Figure 11-18 shows the schematics for the COMPAQ Video Display Controller Board. COMPAQ Computer Corporation does not guarantee the accuracy of the schematics. They are provided to aid in a general understanding of the system operation.



NOTES UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE EITHER 1/4W, 5% OR 1/8W, 1% AND ARE IN OHMS.
2. ALL CAPACITORS ARE 50V AND ARE IN MICROFARADS.
3. COMPONENTS NOT INSTALLED: J1, J2, J4, J6-J10, R1-R4.

REVISIONS			APPROVALS			
REV	ECN NO.	DESCRIPTION OF CHANGE	DATE	DFTG.	ENGR.	REL.
AX	3328	PRE-PRODUCTION RELEASE	6-25-85			
A	4368	**RELEASED FOR PRODUCTION**	10-23-85		KMM	
B	5882	**ADD J11. SWAP U16 PINS 5-9; 41-44. LOC 986; INVERTING BUFFER WAS U1 (805)**	5/8/86			

U11
THIS IS AN UNUSED I.C. POSITION ON THE PCB

NOT POPULATED

Figure 11-18. Video Display Controller Board Schematics (Page 1 of 7)

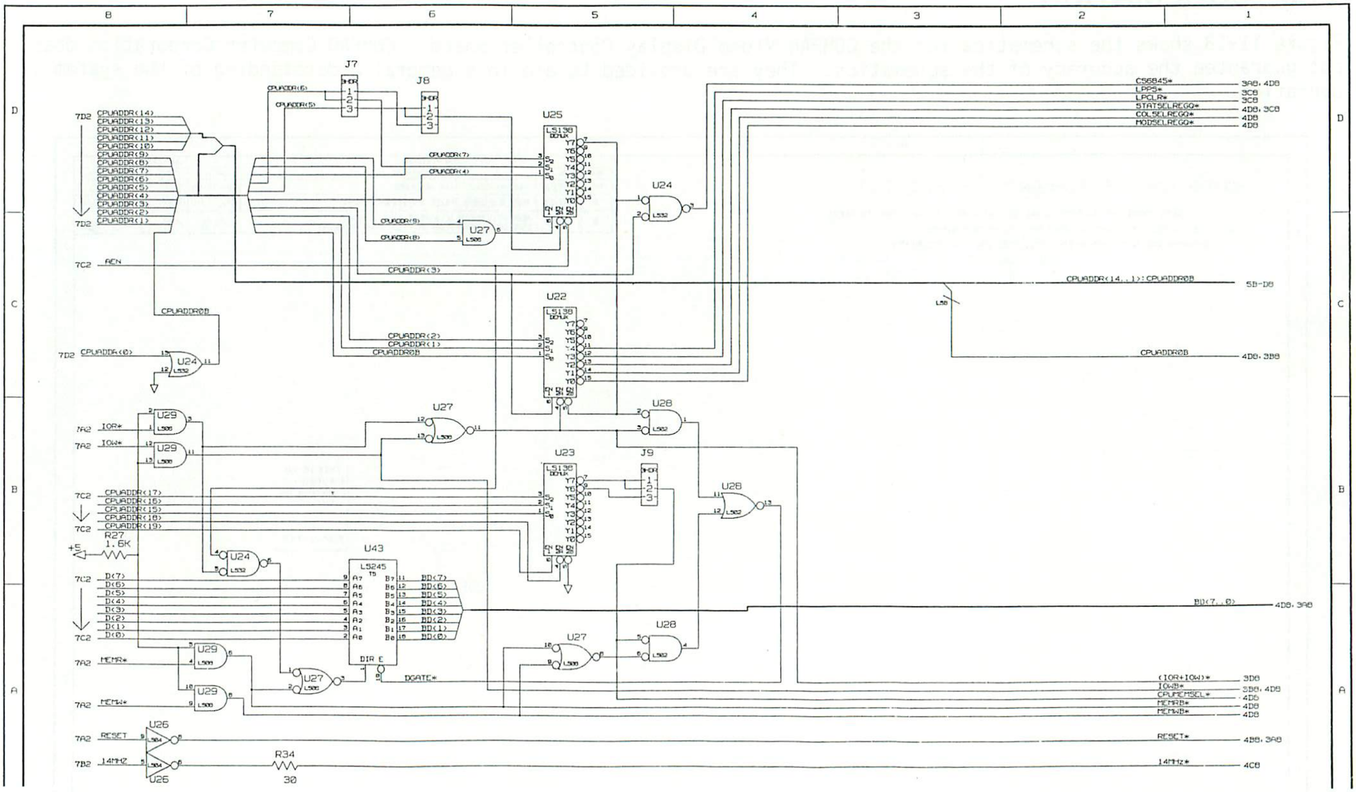


Figure 11-18. Video Display Controller Board Schematics (Page 2 of 7)

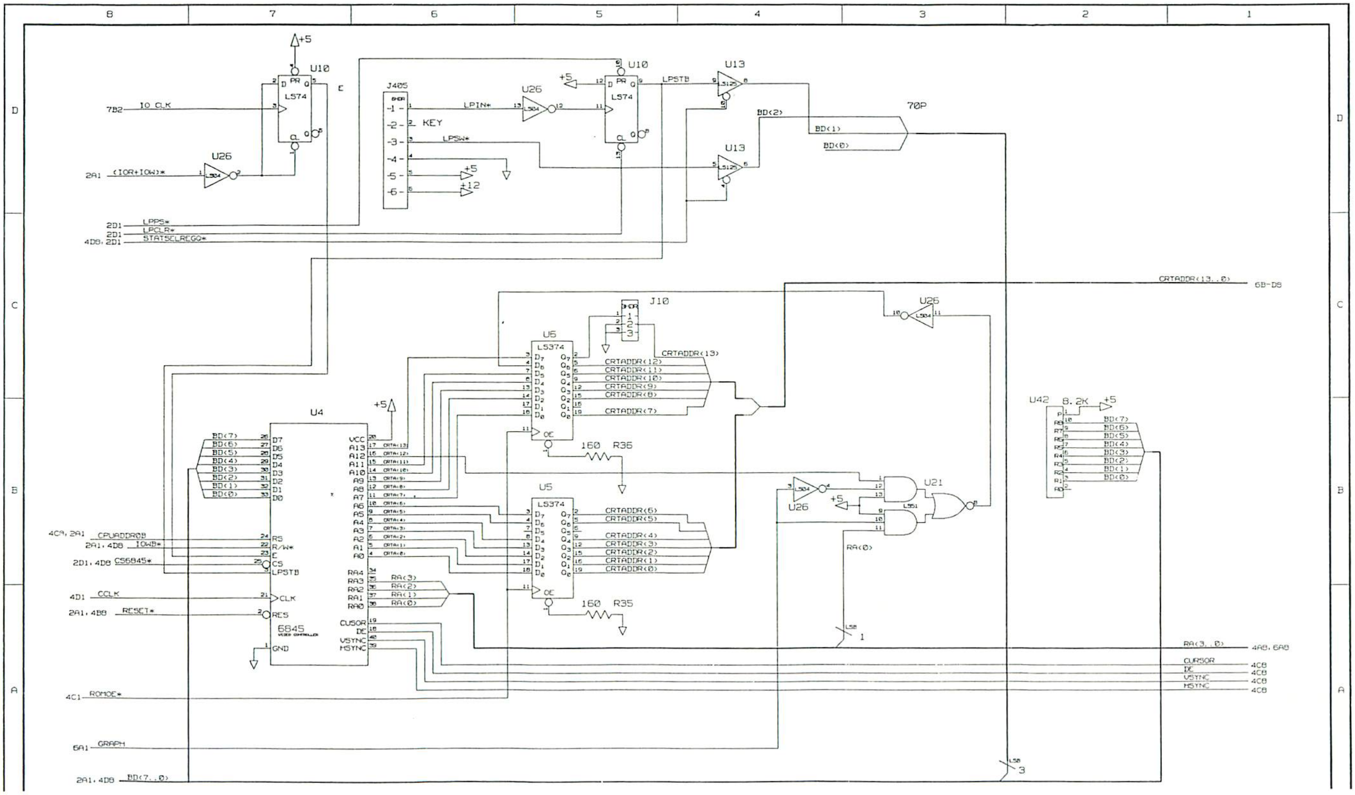


Figure 11-18. Video Display Controller Board Schematics (Page 3 of 7)

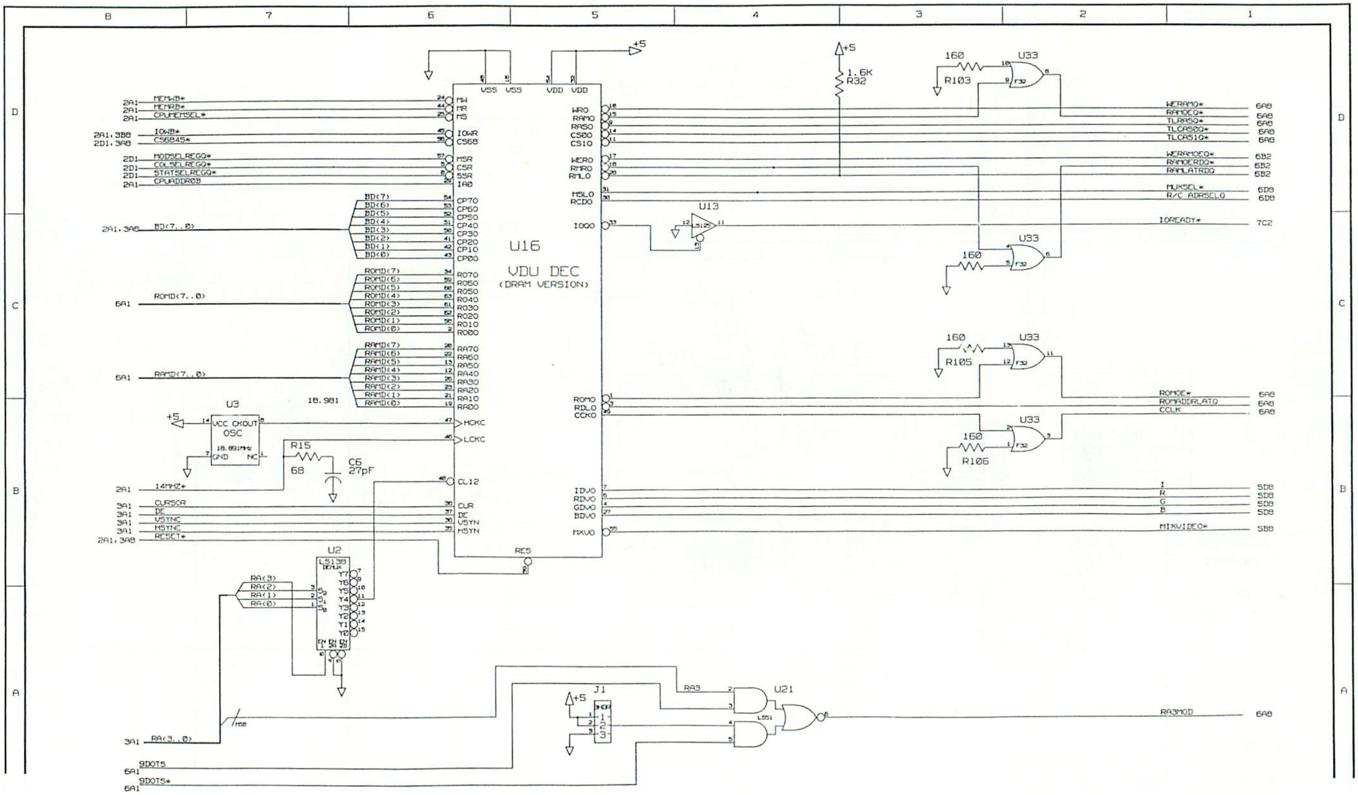


Figure 11-18. Video Display Controller Board Schematics (Page 4 of 7)

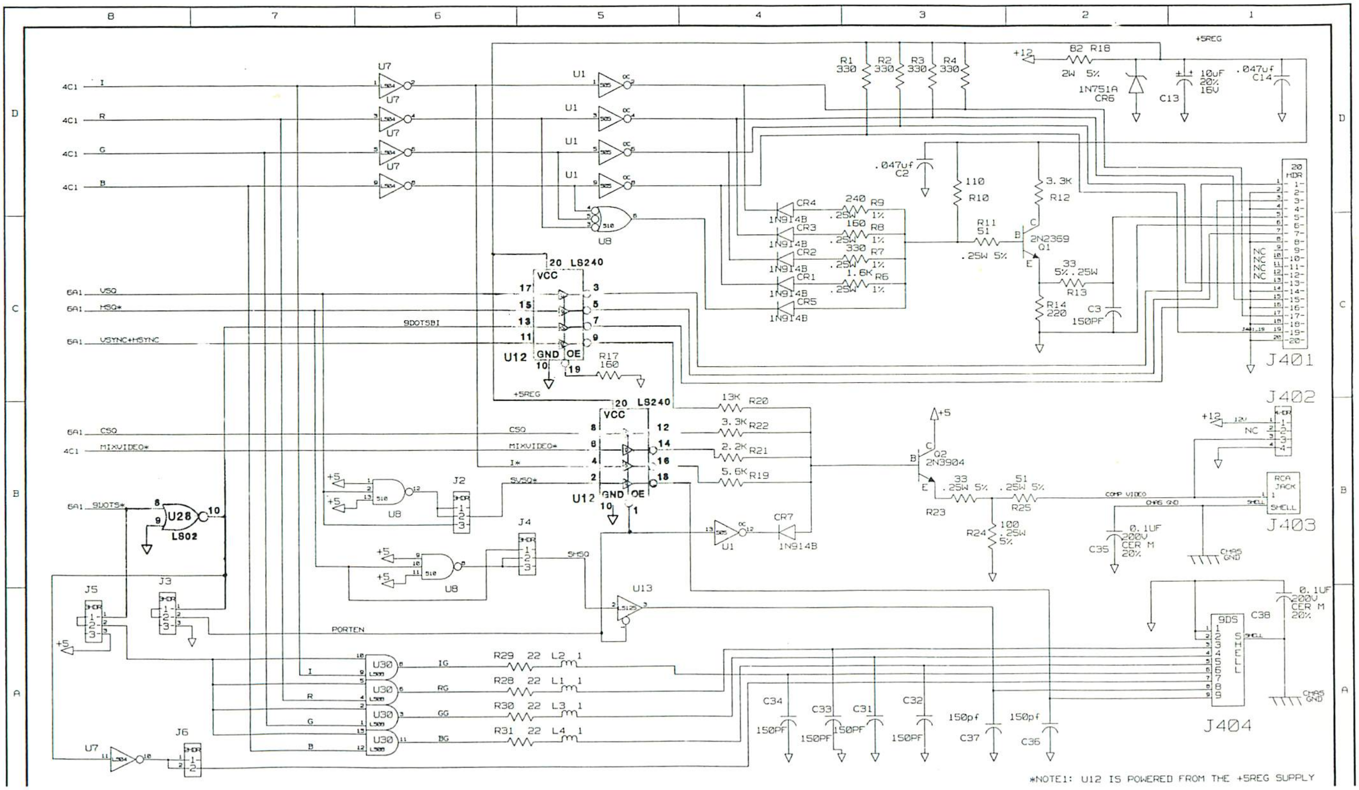


Figure 11-18. Video Display Controller Board Schematics (Page 5 of 7)

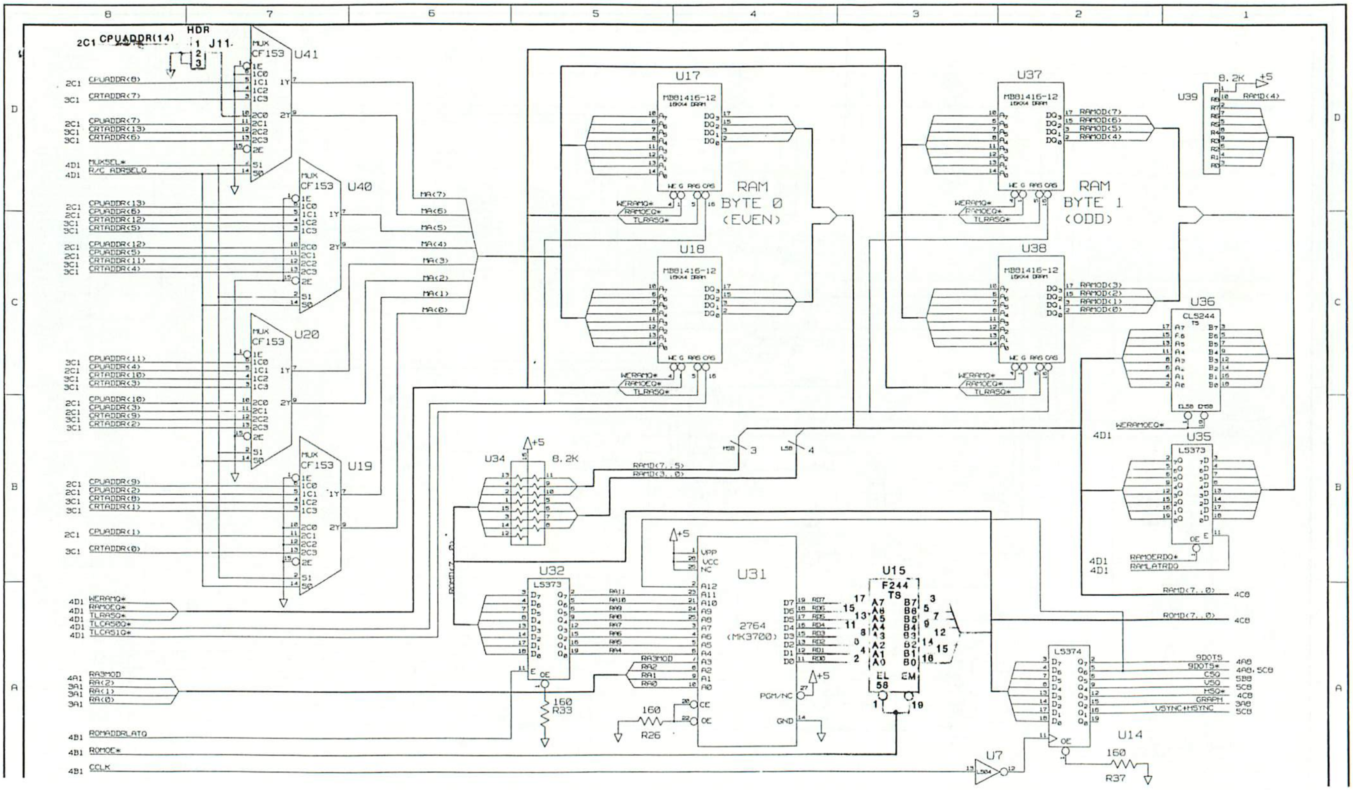


Figure 11-18. Video Display Controller Board Schematics (Page 6 of 7)

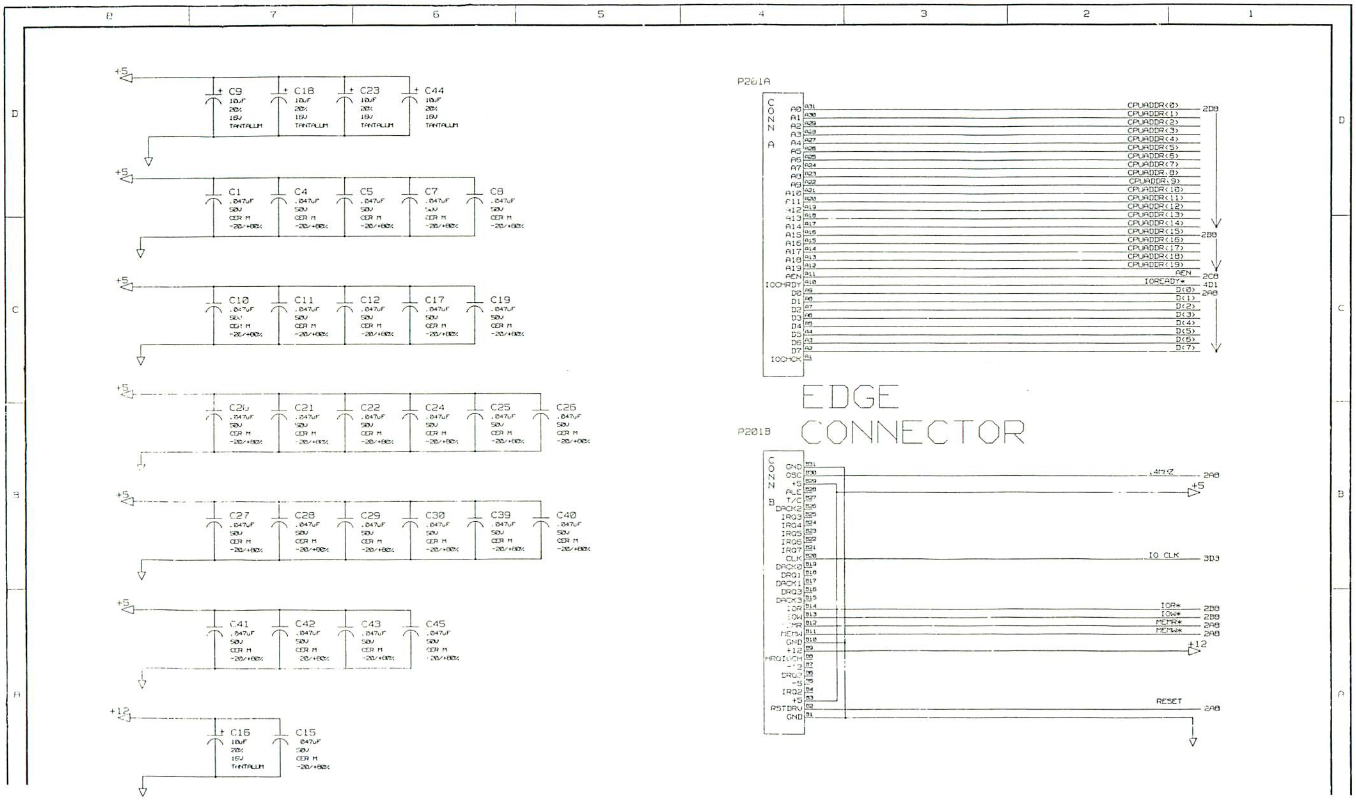


Figure 11-18. Video Display Controller Board Schematics (Page 7 of 7)

Chapter 12
MONITORS

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CHAPTER 12
MONITORS

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Chapter 12
MONITORS

12.1 INTRODUCTION

The COMPAQ Color Monitor and the COMPAQ Dual-Mode Monitor are the two monitors offered for the COMPAQ DESKPRO 386.

12.2 COMPAQ COLOR MONITOR

The COMPAQ Color Monitor, shown in Figure 12-1, is a dual-frequency, high-quality color monitor that supports the COMPAQ Enhanced Color Graphics Board and the COMPAQ Video Display Controller Board. With the COMPAQ Enhanced Color Graphics Board the monitor can display up to 64 colors, using a 6-bit color definition.

The dual-frequency feature allows the monitor to function at two horizontal frequencies. The 15.7-kHz horizontal sweep frequency generates 200 visible (or active) scan lines per vertical frame. The 21.8-kHz horizontal sweep frequency generates 350 visible (or active) scan lines per vertical frame.

Figure 12-2 is a functional block diagram of the COMPAQ Color Monitor.

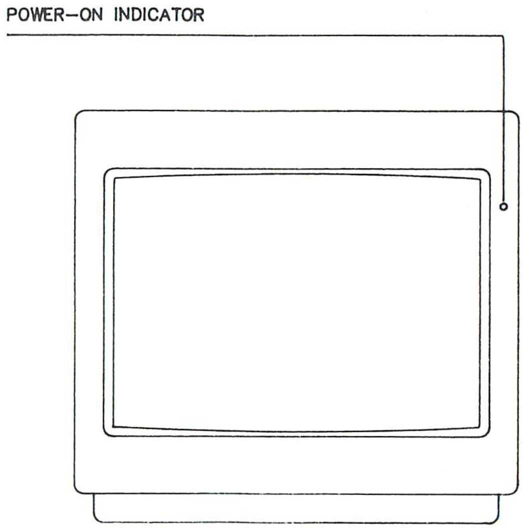


Figure 12-1. COMPAQ Color Monitor

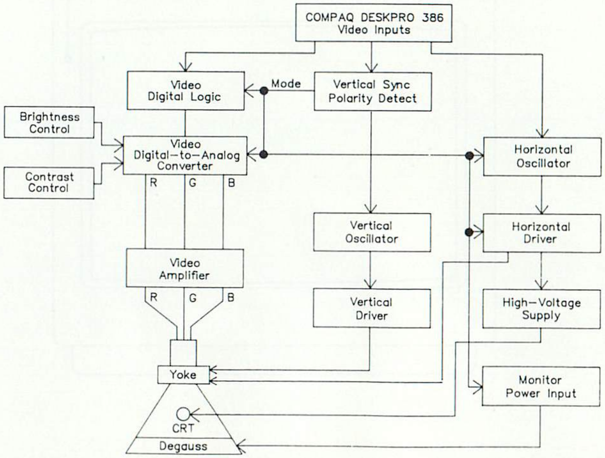


Figure 12-2. COMPAQ Color Monitor Functional Block Diagram

Specifications

Table 12-1 lists the COMPAQ Color Monitor specifications.

Table 12-1. COMPAQ Color Monitor Specifications

Monitor:	
Height	12 in. (30.4 cm)
Depth	15 in. (38.0 cm)
Width	13 in. (35.4 cm)
Weight	28 lb. (12.8 kg)
Display:	
640 pixels x 350 scan lines (64 colors)	
640 pixels x 200 scan lines (16 colors)	
13-in. screen (diagonal)	
90-degree deflection	
Signal Cable:	
Length	60 in. (1.5 m)
Interface	RGBI/RrGgBb using shielded 9-pin subminiature D-type connector
Power:	
Cable Length	60 in. (1.5 m)
Cable Connector	NEMA 5-15P (parallel blade plug, North American units only)
Voltage:	
North American units	120 VAC (60 Hz)
International units	220-240 VAC (50 to 60 Hz)
Power Consumption	100 w (maximum)
Environmental Requirements:	
Temperature:	
Operating	50°F to 104°F (10°C to 40°C)
Nonoperating	14°F to 131°F (-10°C to 55°C)
Humidity	10% to 95% (noncondensing)
Altitude	Mean sea level to 7000 ft. (2 100 m)

Installation Considerations

Adjustable Tilt Bar

The bottom of the monitor has a tilt bar that allows the monitor to be viewed in three positions: level and 5°- or 10°-angled views.

To adjust the tilt bar, gently set the monitor on its left side, push the spring-loaded tilt bar down and set it as desired. Then release the tilt bar and lock it into place.

Video Display Controller Compatibility

Connect the COMPAQ Color Monitor only to a video display controller board having standard RGBI or RrGgBb video outputs with a horizontal frequency output of 15.7 kHz or 21.8 kHz. The COMPAQ Color Monitor works with either the COMPAQ Enhanced Color Graphics Board or the COMPAQ Video Display Controller Board. When the monitor is connected to a video display controller board with incompatible video output signals, the display image, shape, and position may be distorted.

Note: The switch settings on the video display controller board may need to be changed before the COMPAQ Color Monitor functions correctly. (See your video display controller board operations guide for the correct switch settings for the COMPAQ Color Monitor.)

Connecting AC Power

For the North American units of the COMPAQ Color Monitor, the alternating-current (AC) power cable is an integral part of the monitor. To connect the monitor to AC power, plug the power cable into a standard 120-VAC (60-Hz) outlet.

For the International units of the COMPAQ Color Monitor, the AC power cable is a separate cable that must be plugged in to both the monitor and the AC outlet. Connect the "monitor end" of the power cable to the connector on the back of the monitor. Plug the "AC end" of the power cable into the AC outlet. International units operate on 220- to 240-VAC, 50- to 60-Hz power.

Controls

Figure 12-3 shows the following COMPAQ Color Monitor controls:

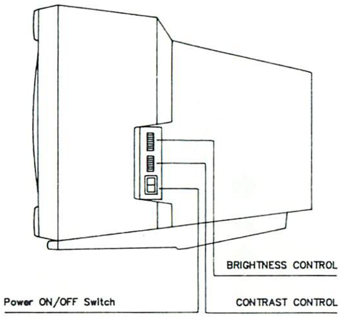
- Power ON/OFF Switch. The Power ON/OFF Switch turns on and off the monitor's AC power. Push the top of the "rocker-type" switch to turn on the monitor. Push the bottom of the switch to turn off the monitor.

- Contrast Control. The Contrast Control adjusts the difference in the degree of brightness among the colors. To increase the contrast, rotate the Contrast Control downward. To decrease the contrast, rotate the Contrast Control upward. The contrast control is not operative in 350 scan-line modes.
- Brightness Control. The Brightness Control adjusts the brightness of the display. To increase the brightness, rotate the Brightness Control downward. To decrease the brightness, rotate the Brightness Control upward.
- Vertical-Height, High-Frequency Mode Control (V-Height-H). The V-Height-H Control adjusts the screen size for the 350 scan-line modes. Adjust this control when you are in any of the 350 scan-line modes until the display height is suitable.
- Vertical-Height, Low-Frequency Mode Control (V-Height-L). The V-Height-L Control adjusts the screen size for the 200 scan-line modes. Adjust this control when you are in any of the 200 scan-line modes until the display height is suitable.

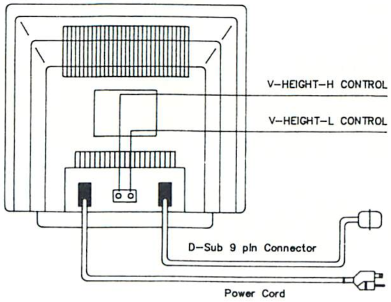
WARNING

DO NOT ATTEMPT TO ADJUST ANY INTERNAL CONTROLS:

1. **REMOVING THE COVER OF THE MONITOR EXPOSES YOU TO DANGEROUS VOLTAGES.**
2. **IMPROPER ADJUSTMENT OF THE INTERNAL CONTROLS CAN PERMANENTLY DAMAGE THE MONITOR.**
3. **ATTEMPTING TO ADJUST THE CONTROLS VOIDS THE WARRANTY ON THE MONITOR.**



Right-Side View



Rear View

Figure 12-3. COMPAQ Color Monitor Controls

Self-Test

The COMPAQ Color Monitor has a self-test system. To perform this self-test:

1. Turn off the monitor.
2. Disconnect the monitor signal cable from the computer.
3. Turn on the monitor and look at the screen. The screen color will be white if the monitor is working properly after warm up.

If the screen is dark or any color other than white, contact your Authorized COMPAQ Computer Dealer for service.

Connectors

The COMPAQ Color Monitor has one signal connector, which is shown in Figure 12-4. The monitor interprets the video signal function according to the polarity of the vertical sync (VS) signal coming from the video display controller board. When the VS signal is active high (+ polarity), the monitor operates in the 200 scan-line mode. When the VS signal is active low (- polarity), the monitor operates in the 350 scan-line mode.

Table 12-2 lists the monitor connector signal descriptions. Figures 12-5 and 12-6 show the timing parameters for the COMPAQ Color Monitor.

Table 12-2. Monitor Connector Signal Descriptions

Pin	200 Scan-line Description	350 Scan-line Description
1	Signal Ground	Signal Ground
2	Not used	r-secondary red
3	R-red	R-primary red
4	G-green	G-primary green
5	B-blue	B-primary blue
6	I-intensity	g-secondary green
7	Not-used	b-secondary blue
8	HS-horizontal sync	HS-horizontal sync
9	VS-vertical sync	VS-vertical sync

Note: All signals are active-high TTL signals, except the VS signal. Polarity of VS determines the number of scan lines.

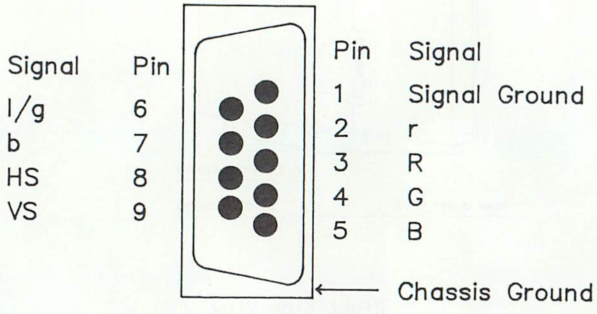
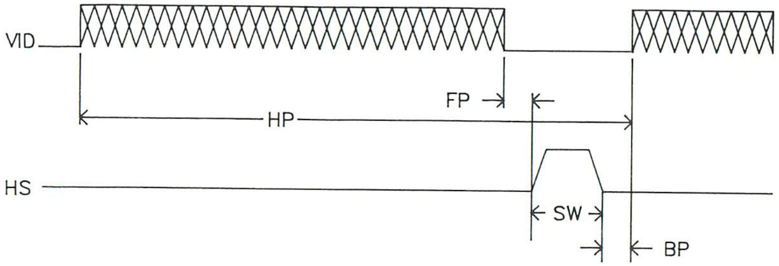
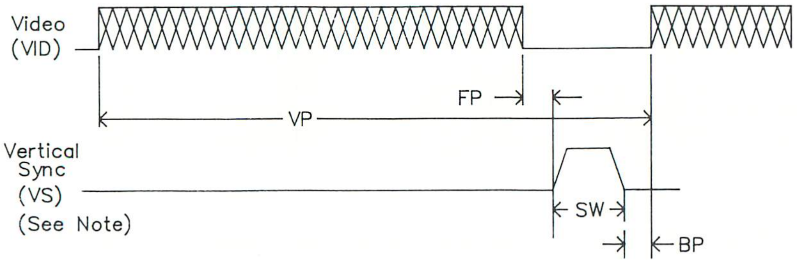


Figure 12-4. COMPAQ Color Monitor Signal Connector



Symbol	Parameter	350 Scan lines	200 Scan lines
HP	Horizontal Period	45.8 μs	63.7 μs
FP	Front Porch	0 μs	6.7 μs
SW	Sync Width	4.9 μs	4.5 μs
BP	Back Porch	1.5 μs	7.8 μs

Figure 12-5. COMPAQ Color Monitor Horizontal Timing



Symbol	Parameter	350 Scan lines	200 Scan lines
VP	Vertical Period	16.70 ms	16.80 ms
FP	Front Porch	0.00 ms	1.53 ms
SW	Sync Width	0.60 ms	0.19 ms
BP	Back Porch	0.08 ms	2.23 ms

Note: VS is active low for the 350 scan line mode.
VS is active high for the 200 scan line mode.

Figure 12-6. COMPAQ Color Monitor Vertical Timing

12.3 COMPAQ DUAL-MODE MONITOR

The COMPAQ Dual-Mode Monitor is a monochrome, dual-frequency monitor for use with the COMPAQ Video Display Controller Board or the COMPAQ Enhanced Color Graphics Board.

Figure 12-7 shows the COMPAQ Dual-Mode Monitor.

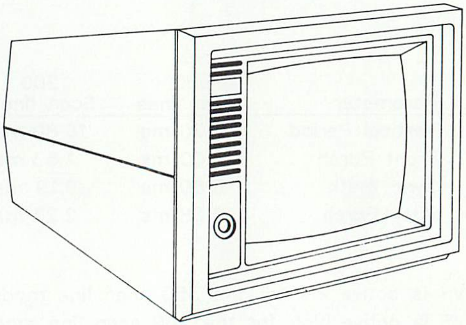


Figure 12-7. COMPAQ Dual-Mode Monitor

Figure 12-8 is the functional block diagram for the COMPAQ Dual-Mode Monitor.

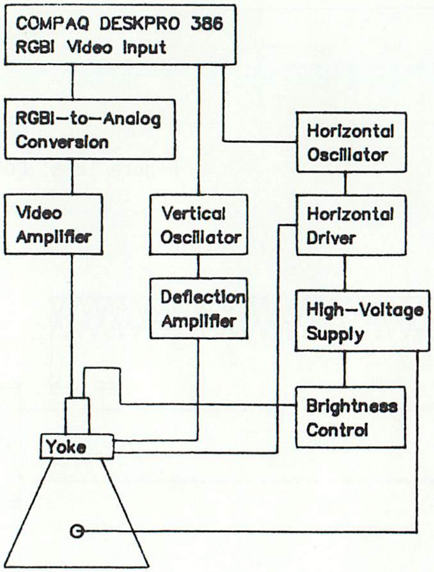


Figure 12-8. COMPAQ Dual-Mode Monitor Functional Block Diagram

Specifications

Table 12-3 lists the COMPAQ Dual-Mode Monitor specifications.

Table 12-3. COMPAQ Dual-Mode Monitor Specifications

Screen:	
CRT size	12 in. diagonal
Phosphor	Green, medium persistence or Amber, medium persistence
Active area (see Figure 12-7)	
Horizontal	8.1 in. (20.6 cm)
Vertical	6.0 in. (15.2 cm)
Power Requirements:	
Voltage	12.4 Vdc, ±4%
Current	1.8 A, maximum 2.5-A surge (10 ms)
Signals:	
Video	Digital, TTL-level RGBI yielding 15 levels of intensity
Horizontal Sync	Positive, TTL-level
Vertical Sync	Positive, TTL-level
Connectors:	
Power	3-pin male circular DIN AMP 211502-5, or equiv.
Signal	9-pin male subminiature D

Figure 12-9 shows the active area on the screen.

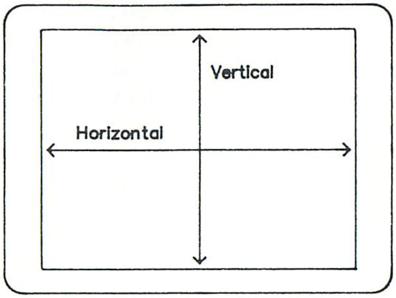


Figure 12-9. Active Screen Area

Video Display Controller Compatibility

Connect the COMPAQ Dual-Mode Monitor only to a COMPAQ Video Display Controller Board. The COMPAQ Dual-Mode Monitor works with either the COMPAQ Video Display Controller Board or the COMPAQ Enhanced Color Graphics Board.

The COMPAQ Dual-Mode Monitor supports two different display modes with different scanning frequencies for each mode. The high-scan mode has a horizontal scan frequency of 18.5 kHz and a vertical scan frequency of 50 Hz, non-interlaced. High scan supports the text modes, using a 9 x 14-pixel character block. This mode has 350 active vertical lines for 25 rows of 14-pixel-high characters, and 720 horizontal pixels for 80 columns of 9-pixel-wide characters. The high-scan mode is used by the COMPAQ Video Display Controller Board to generate high-resolution text while also providing compatibility with software products developed for color graphics adapters (CGA).

When used with the COMPAQ Enhanced Color Graphics Board, the Dual-Mode Monitor provides 15 levels of intensity to simulate the 64 colors that would be displayed on the COMPAQ Color Monitor. The dual-mode monitor also provides high-resolution text with this board. Table 12-4 lists the different functions supported by the dual-mode monitor with the COMPAQ Video Display Controller Board and the COMPAQ Enhanced Color Graphics Board.

Table 12-4. Dual-Mode Monitor Functions

Video Display Controller:	
Mode	Format
Text	720 x 350
Graphics	640 x 200
Enchanced Color Graphics Board:	
Mode	Format
Mono Text	720 x 350
Mono Graph	640 x 350
Color Text	640 x 350
Enhanced Graphics	640 x 350
Compatible Graphics	640 x 200

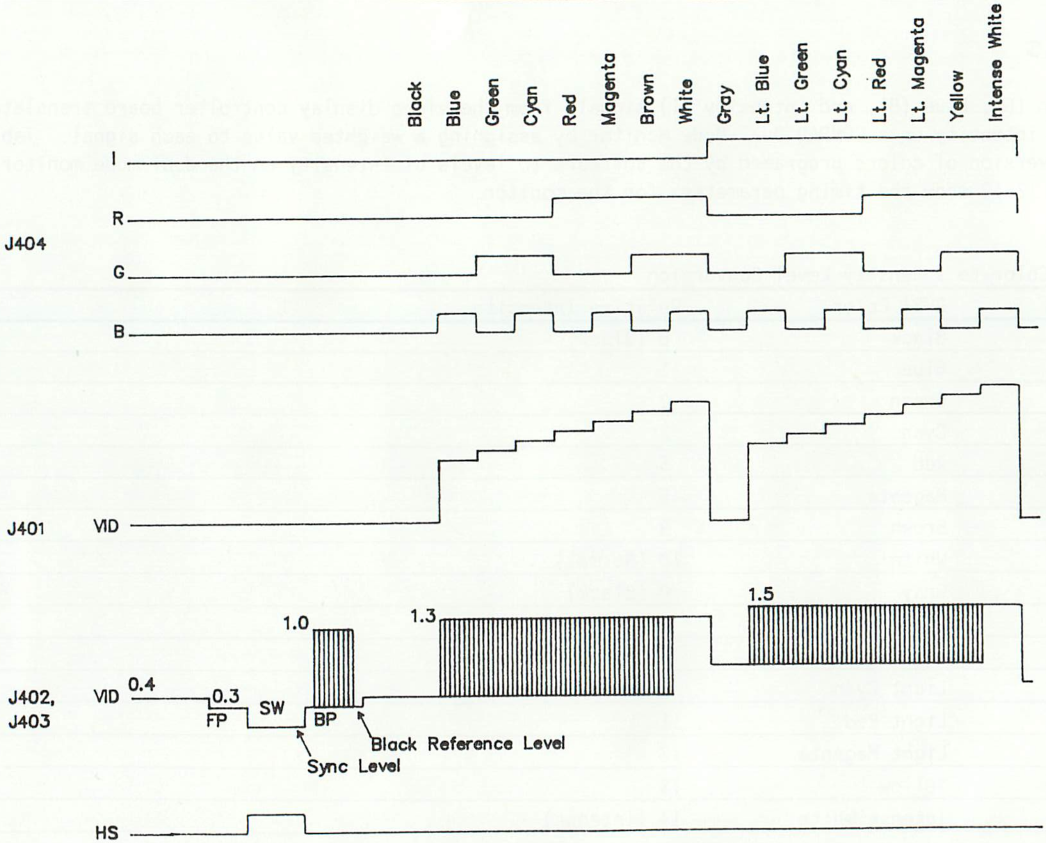
Note: The switch settings on the video board may need to be changed before the COMPAQ Dual-Mode Monitor functions correctly. (See your video board operations guide for the correct switch settings for the COMPAQ Dual-Mode Monitor.)

Waveforms

Red (R), green (G), blue (B), and intensity (I) signals from the video display controller board translate to variations in intensity on a COMPAQ Dual-Mode Monitor by assigning a weighted value to each signal. Table 12-5 shows the conversion of colors programed by the software to levels of intensity on the dual-mode monitor. Figures 12-10 through 12-12 show the timing parameters for the monitor.

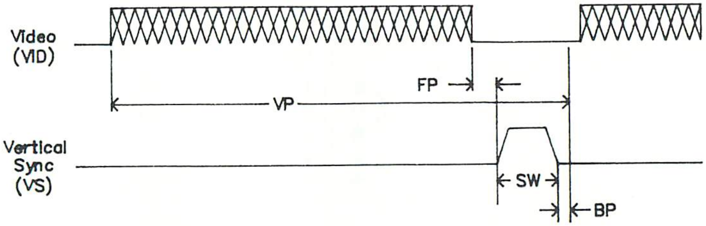
Table 12-5. Color to Intensity Level Conversion

R	G	B	I	RGBI Color	Relative Intensity
0	0	0	0	Black	0 (Black)
0	0	1	0	Blue	1
0	1	0	0	Green	2
0	1	1	0	Cyan	3
1	0	0	0	Red	5
1	0	1	0	Magenta	6
1	1	0	0	Brown	9
1	1	1	0	White	10 (Normal)
0	0	0	1	Gray	0 (Black)
0	0	1	1	Light Blue	4
0	1	0	1	Light Green	7
0	1	1	1	Light Cyan	8
1	0	0	1	Light Red	11
1	0	1	1	Light Magenta	12
1	1	0	1	Yellow	13
1	1	1	1	Intense White	14 (Intense)



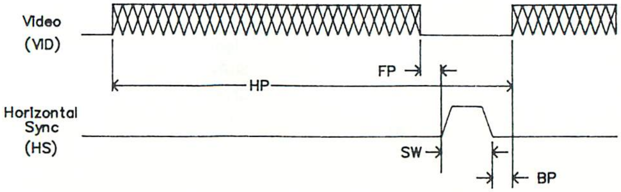
Notes: 1. Burst is only present in the 40 x 25 text mode or the 320 x 200 graphics mode.
2. This is a block–frame format without equalization pulses.

Figure 12-10. Video Timing Waveforms



Symbol	Parameter	High Scan	Low Scan
VP	Vertical Period	20.00 ms	16.68 ms
FP	Front Porch	0.00 ms	1.53 ms
SW	Sync Width	0.16 ms	0.19 ms
BP	Back Porch	0.92 ms	2.23 ms

Figure 12-11. COMPAQ Dual-Mode Monitor Horizontal Timing



Symbol	Parameter	High Scan	Low Scan
HP	Horizontal Period	54.1 μs	63.7 μs
FP	Front Porch	5.7 μs	6.7 μs
SW	Sync Width	3.8 μs	4.5 μs
BP	Back Porch	6.6 μs	7.8 μs

Figure 12-12. COMPAQ Dual-Mode Monitor Vertical Timing

Connectors

The dual-mode monitor signal cable connects to the RGBI connector (J404) on the COMPAQ Video Display Controller Board or COMPAQ Enhanced Color Graphics Board. The dual-mode monitor power cable connects to the monitor power receptacle. These connectors are located on the back of the system. Figure 12-13 and Table 12-6 describe the monitor signal connector. Figure 12-14 shows the monitor power connector.

Table 12-6. Dual-Mode Monitor Connector Signal Description

Signal	Pin	I/O	Description
B	5	I	Blue
G	4	I	Green
HS	8	I	Horizontal sync
I	6	I	Intensity
MODE	7	I	Controls the monitor high- or low-scan mode. During a mode change, both horizontal and vertical sync are suppressed for up to 16 vertical frames. The MODE signal is high for the low-scan mode and low for the high-scan mode.
R	3	I	Red
Signal Ground	1,2	-	TTL-signal reference
VS	9	I	Vertical sync

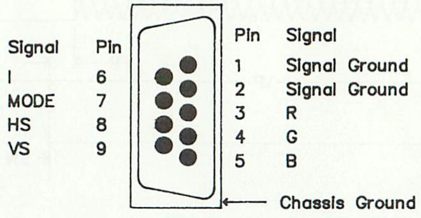


Figure 12-13. COMPAQ Dual-Mode Monitor Connector Pinout

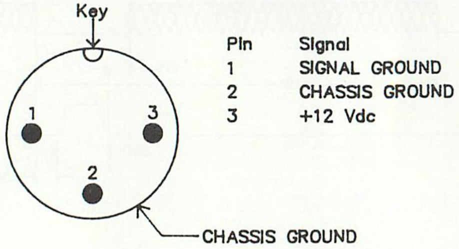


Figure 12-14. COMPAQ Dual-Mode Monitor Power Connector Pinout

Appendix A
ERROR MESSAGES

Appendix A
ERROR MESSAGES

ERROR MESSAGES

The following pages list the error codes and a brief description of the probable source of the error.

Common Power-On Messages

Table A-1 lists the messages that could occur when the system is turned on or reset.

Table A-1. Power-On Messages

Message	Beeps	Probable Cause
163-Time & Date Not Set	2S	Invalid Time
(One very short beep)	1VS	Power-up Successful; FAST (8 MHz) Speed
(Two very short beeps)	2VS	Power-up Successful; System-board DIP Switch Selected Speed (HIGH or AUTO)
RESUME = "F1" KEY	None	Any Failure

Initialization Diagnostic Messages

Table A-2 lists error messages that may occur as part of the Power-On Self-Test (POST).

Table A-2. Power-On Self-Test (Post) Messages

Message	Beeps	Probable Cause
101-I/O ROM Error	1L, 1S	Option ROM checksum
101-ROM Error	1L, 1S	System ROM checksum
102-System Board Failure	None	DMA, timers, etc.
102-System or Memory Board Failure	None	High-order addresses
162-System Options Error	2S	No diskette drives or mismatch in drive types
162-System Options Not Set-(Run Setup)	2S	System configuration
164-Memory Size Error	2S	Memory size discrepancy
XX000Y ZZ 201-Memory Error	None	RAM failure
XX000Y ZZ 203-Memory Address Error	2S	Memory high address error
301-Keyboard Error	None	Keyboard failure
301-Keyboard Error or Test Fixture Installed	None	Keyboard test fixture
302-System Unit Security Lock is Locked - Unlock System Unit Security Lock	2S	System locked
303-Keyboard Controller Error	None	Keyboard controller
304-Keyboard or System Unit Error	None	Keyboard interface
402-Monochrome Adapter Failure	1L, 2S	Mono display controller
501-Display Adapter Failure	1L, 2S	Graphics display controller
601-Diskette Controller Error	None	Diskette controller
602-Diskette Boot Record Error	None	Diskette does not have a valid boot record
702-Coprocessor Detection Error	None	Switch setting does not agree with 80287 detection
1780-Disk 0 Failure	None	Fixed disk drive 0 not ready
1781-Disk 1 Failure	None	Fixed disk drive 1 not ready
1782-Disk Controller Failure	None	Fixed disk drive controller
1790-Disk 0 Error	None	Fixed disk drive 0 access error
1791-Disk 1 Error	None	Fixed disk drive 1 access error
Parity Check 2 XX000Y ZZ	None	Parity RAM failure

Notes: 1. Tables A-13, A-14, and A-15 define XX, Y, and ZZ.
2. L means a long beep, and S means a short beep.

Advanced Diagnostics Error Messages

The following tables list error messages that may occur during testing by the advanced diagnostics.

Processor

Table A-3 lists error messages that relate to the 80386 microprocessor or to other system board devices.

Table A-3. Processor Error Message

Message	Problem Failure
101-01	CPU test failed
101-02	32-bit CPU test failed
102-01	Numeric coprocessor initial status word incorrect
102-02	Numeric coprocessor initial control word incorrect
102-03	Numeric coprocessor tag word not all ones
102-04	Numeric coprocessor tag word not all zeros
102-05	Numeric coprocessor exchange command failed
102-06	Numeric coprocessor masked exception incorrectly handled
102-07	Numeric coprocessor unmasked exception incorrectly handled
102-08	Numeric coprocessor wrong mask bit set in status register
102-14	Switch indicates no numeric coprocessor present
102-15	Numeric coprocessor is inoperative or socket is unoccupied
103-01	DMA page registers test failed
103-02	DMA byte controller test failed

(Continued)

Table A-3. Processor Error Messages

Message	Problem Failure
103-03	DMA word controller test failed
104-01	Interrupt controller master test failed
104-02	Interrupt controller slave test failed
104-03	Interrupt controller software RTC is inoperative
105-01	Port 61 bit 6 not at zero
105-02	Port 61 bit 5 not at zero
105-03	Port 61 bit 3 not at zero
105-04	Port 61 bit 1 not at zero
105-05	Port 61 bit 0 not at zero
105-06	Port 61 bit 5 not at one
105-07	Port 61 bit 3 not at one
105-08	Port 61 bit 1 not at one
105-09	Port 61 bit 0 not at one
105-10	Port 61 I/O test failed
105-11	Port 61 bit 7 not at zero
105-12	Port 61 bit 2 not at zero
105-13	No interrupt generated by failsafe timer
105-14	NMI not triggered by failsafe timer
106-01	Keyboard controller self-test failed
107-01	CMOS RAM test failed
108-02	CMOS interrupt test failed
108-03	CMOS interrupt test, CMOS not properly initialized
109-01	CMOS clock load data test failed
109-02	CMOS clock rollover test failed
109-03	CMOS clock test, CMOS not properly initialized
110-01	Programmable timer load data test failed
110-02	Programmable timer dynamic test failed

(Continued)

Table A-3. Processor Error Messages (Concluded)

Message	Probable Failure
110-03	Program timer 2 load data test failed
111-01	Refresh detect test failed
112-01	Speed test slow mode out of range
112-02	Speed test mixed mode out of range
112-03	Speed test fast mode out of range
112-04	Speed test unable to enter slow mode
112-05	Speed test unable to enter mixed mode
112-06	Speed test unable to enter fast mode
112-07	Speed test system error
112-08	Unable to enter auto mode in speed test
112-09	Unable to enter high mode in speed test
112-10	Speed test high mode out of range
112-11	Speed test auto mode out of range
112-12	Speed test variable speed mode inoperative
113-01	Protected mode test failed
114-01	Speaker test failed
199-00	Installed devices test failed

Memory

Table lists A-4 error messages for memory-related errors.

Table A-4. Memory Error Messages

Message	Probable Failure
201-01	Memory machine ID test failed
202-01	Memory system ROM checksum failed
202-02	Failed RAM/ROM map test
202-03	Failed RAM/ROM protect test
203-01	Memory write/read test failed
203-02	Error during saving program memory in write/read test
203-03	Error during restore of program memory in write/read test
204-01	Memory address test failed
204-02	Error during saving program memory in address test
204-03	Error during restore of program memory in address test
204-04	A20 address test failed
204-05	Page hit address test failed
205-01	Walking I/O test failed
205-02	Error during saving program memory in walking I/O test
205-03	Error during restore of program memory in walking I/O test

Keyboard

Table A-5 lists error messages for keyboard-related errors.

Table A-5. Keyboard Error Messages

Message	Probable Failure
301-01	Keyboard short test, 8042 self-test failed
301-02	Keyboard short test, interface test failed
301-03	Keyboard short test, echo test failed
301-04	Keyboard short test, keyboard reset failed
301-05	Keyboard short test, keyboard reset failed
302-01	Keyboard long test, failed
303-01	Keyboard LED test, 8042 self-test failed
303-02	Keyboard LED test, reset test failed
303-03	Keyboard LED test, reset failed
303-04	Keyboard LED test, LED command test failed
303-05	Keyboard LED test, LED command test failed
303-06	Keyboard LED test, LED command test failed
303-07	Keyboard LED test, LED command test failed
303-08	Keyboard LED test, command byte restore test failed
303-09	Keyboard LED test, LEDs failed to light
304-01	Keyboard repeat key test failed
304-02	Unable to enter mode 3
304-03	Incorrect scan code from keyboard
304-04	No make code observed
304-05	Unable to disable repeat key feature
315-01	Security lock inoperative
315-02	Security lock stuck in locked position

Printer

Table A-6 lists error messages for printer-related errors.

Table A-6. Printer Error Messages

Message	Probable Failure
401-01	Printer failed or not connected
402-01	Printer data register failed
402-02	Printer control register failed
402-03	Printer data and control register failed
402-04	Printer loopback failed
402-05	Printer loopback and data register failed
402-06	Printer loopback and control register failed
402-07	Printer loopback, data and control reg failed
402-08	Printer interrupt test failed
402-09	Printer interrupt and data register failed
402-10	Printer interrupt and control register failed
402-11	Printer interrupt, data and control register failed
402-12	Printer interrupt and loopback failed
402-13	Printer interrupt, loopback, data reg failed
402-14	Printer interrupt, loopback, ctrl reg failed
402-15	Printer interrupt, loopback, data, and control, and register failed
402-16	Printer unexpected interrupt received
403-01	Printer pattern test failed
498-00	Printer failed or not connected

Video

Table A-7 lists error messages for video-related errors.

Table A-7. Video Error Messages

Message	Probable Failure
501-01	Video controller test failed
502-01	Video memory test failed
503-01	Video attribute test failed
504-01	Video character set test failed
505-01	Video 80X25 mode 9X14 char cell test failed
506-01	Video 80X25 mode 8X8 char cell test failed
507-01	Video 40X25 mode test failed
508-01	Video 320X200 mode color set 0 test failed
509-01	Video 320X200 mode color set 1 test failed
510-01	Video 640X200 mode test failed
511-01	Video screen memory page test failed
512-01	Video gray scale test failed
514-01	Video white screen test failed
516-01	Video noise pattern test failed
517-01	Lightpen text mode test failed - no response
517-02	Lightpen text mode test failed - invalid response
517-03	Lightpen medium resolution mode test failed - no response
517-04	Lightpen medium resolution mode test failed - invalid response

Diskette Drive

Table A-8 lists error messages for diskette-related errors.

Table A-8. Diskette Drive Error Messages

Message	Probable Failure
600-xx	Floppy ID drive types test
601-xx	Floppy format
602-xx	Floppy read test
603-xx	Floppy write/read/compare test
604-xx	Floppy random seek test
605-xx	Floppy ID media test
606-xx	Floppy speed test
607-xx	Floppy wrap test
608-xx	Floppy write-protect test
609-xx	Floppy reset controller test
610-xx	Floppy change line test
-xx	
01	Exceeded maximum soft error limit
02	Exceeded maximum hard error limit
03	Previously exceeded max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read/compare
09	Failed to format a track

Table A-8. Diskette Drive Error Messages (Concluded)

Message	Probable Failure
-xx	
10	Failed sector wrap test
20	Failed to get drive type
21	Failed to get change line status
22	Failed to clear change line status
23	Failed to set drive type in ID media
24	Failed to read media
25	Failed to verify media
26	Failed to read media in speed test
27	Failed speed limits
28	Failed write protect test
694-00	Pin 34 not cut
697-00	Diskette type error
698-00	Diskette drive speed not within limits
699-00	Drive/media ID error - rerun SETUP

Serial Communications

Table A-9 lists error messages for serial communications-related errors.

Table A-9. Serial Communications Error Messages

Message	Probable Failure
1101-01	Serial Port Test, UART DLAB bit failure
1101-02	Serial Port Test, Line input or UART fault
1101-03	Serial Port Test, Address line fault
1101-04	Serial Port Test, Data line fault
1101-05	Serial Port Test, UART control signal failure
1101-06	Serial Port Test, UART THRE bit failure
1101-07	Serial Port Test, UART DATA READY bit failure
1101-08	Serial Port Test, UART TX/RX buffer failure
1101-09	Serial Port Test, INTERRUPT circuit failure
1101-10	Serial Port Test, COM 1 set to interrupt 3
1101-11	Serial Port Test, COM 2 set to interrupt 4
1101-12	Serial Port Test, DRIVE/RECEIVER control signal failure
1101-13	Serial Port Test, UART control signal interrupt failure
1101-14	Serial Port Test, DRIVER/RECEIVER data failure
1109-01	Clock register initialization failure
1109-02	Clock register rollover failure
1109-03	Clock reset failure
1109-04	Input line or clock failure
1109-05	Address line fault
1109-06	Data line fault

Fixed Disk Drive

Table A-10 lists error messages for fixed disk-related errors.

Table A-10. Fixed Disk Drive Error Messages

Message	Probable Failure
1700-xx	Hard disk ID drive types test
1701-xx	Hard disk format test
1702-xx	Hard disk read test
1703-xx	Hard disk write/read/compare test
1704-xx	Hard disk random seek test
1705-xx	Hard disk controller test
1706-xx	Hard disk drive ready test
1707-xx	Hard disk recalibrate test
1708-xx	Hard disk format bad track test
1709-xx	Hard disk reset controller test
1710-xx	Hard disk park head test
1714-xx	Hard disk file write test
1715-xx	Hard disk head select test
1716-xx	Hard disk conditional format test
1717-xx	Hard disk ECC test
-xx	
01	Exceeded maximum soft error limit
02	Exceeded maximum hard error limit
03	Previously exceed max soft error limit
04	Previously exceeded max hard error limit
05	Failed to reset controller
06	Fatal error while reading
07	Fatal error while writing
08	Failed compare of write/read/compare
09	Failed to format a track
10	Failed sector wrap track
40	Failed cylinder 0
41	Drive not ready
42	Recalibrate failed
43	Failed to format track bad
44	Failed hard disk controller diagnostic
45	Failed to get drive parameter from ROM
46	Invalid drive parameters found in ROM
47	Failed to park heads
48	Failed to move disk table to RAM
49	Failed to read media in file write test
50	Failed file I/O in write test
51	Failed file I/O in read test
52	Failed file I/O in compare test
53	Failed drive/head register test
54	Failed digital input register test
55	Failed cylinder 1
56	Controller RAM diagnostics failed
57	Controller to drive test failed
58	Failed to write sector buffer
59	Failed to read sector buffer

(Continued)

Table A-10. Fixed Disk Drive Error Messages (Concluded)

Message	Probable Failure
60	Failed to compare sector buffer
61	Failed uncorrectable error
62	Failed correctable error
63	Failed soft error rate
65	Exceeded max bad sector per track
66	Failed init drive parameter
67	Failed to write long
68	Failed to read long
69	Failed to read drive size from controller
70	Failed translate mode
71	Failed non-translated mode
1799-00	Invalid fixed disk drive type

Fixed Disk Drive Back-Up (Tape)

Table A-11 lists fixed disk drive back-up-related errors.

Table A-11. Error Messages

Message	Probable Cause
1901-xx	Tape servo write
1902-xx	Tape format
1903-xx	Tape drive sensor test
1904-xx	Tape BOT EOT test
1905-xx	Tape read test
1906-xx	Tape write/read/compare test
-xx	
01	Drive not installed
02	Cartridge not installed
03	Tape motion error
04	Drive busy error
05	Track seek error
06	Tape write protected error
07	Tape already servo written
08	Unable to servo write
09	Unable to format
10	Format mode error
11	Drive recalibration error
12	Tape not servo written
13	Tape not formatted
14	Drive timeout error
15	Sensor error flag
16	Block locate (block ID) error
17	Soft error limit exceeded

(Continued)

Table A-11. Fixed Disk Drive Error Messages (Concluded)

Message	Probable Failure
18	Hard error limit exceeded
19	Write (probably ID error)
20	765 fatal error
21	Got servo pulses 2nd time but not 1st
22	Never got to EOT after servo check
25	Unable to erase cartridge
26	Cannot ID drive
27	Drive not compatible with controller
28	Format gap error

Enhanced Color Graphics

Table A-12 lists the Enhanced Color Graphics Controller Board related errors.

Table A-12. Enhanced Color Graphics Error Messages

Message	Probable Failure
2402-01	VDU memory test failed
2403-01	VDU attribute test failed
2404-01	VDU character set test failed
2405-01	VDU 80x25 mode 9x14 char cell test failed
2406-01	VDU 80x25 mode 8x8 char cell test failed
2407-01	VDU 40x25 mode test failed
2408-01	VDU 320x200 mode color set 0 test failed
2409-01	VDU 320x200 mode color set 1 test failed
2410-01	VDU 640x200 mode test failed
2411-01	VDU Screen memory page test failed
2412-01	VDU Gray scale test failed
2414-01	VDU White screen test failed
2416-01	VDU Noise pattern test failed

(Continued)

Table A-12. Enhanced Color Graphics Error Messages (Concluded)

Message	Probable Failure
2417-01	Lightpen text mode test failed - no response
2417-02	Lightpen text mode test failed - invalid response
2417-03	Lightpen medium res. mode test failed - no response
2417-04	Lightpen medium res. mode failed - invalid response
2418-01	ECG memory test failed
2418-02	ECG shadow RAM test failed
2419-01	ECG ROM checksum test failed
2420-01	ECG attribute test failed
2421-01	ECG 640x200 graphics node test failed
2422-01	ECG 640x350 16 color set test failed
2423-01	ECG 640x350 64 color set test failed
2424-01	ECG monochrome text mode test failed
2425-01	ECG monochrome graphics mode test failed

Memory-Error Codes

Memory-error codes result when the system detects a memory fault during the power-on self-test or as a result of a diagnostic test. The test programs attempt to isolate the memory fault to a specific data bit. Refer to the COMPAQ DESKPRO 386 Maintenance and Service Guide for RAM device replacement instructions.

In some cases, replacing the memory device will not solve the problem because: 1) the system may not be able to accurately determine which RAM device or devices is at fault, and 2) the problem may be due to a failure in the memory-support circuitry, not the memory device.

When replacing the suspected defective memory devices does not solve the problem, or when the memory devices are soldered onto the memory board, return your system to an Authorized COMPAQ Dealer for service.

The memory-error code points to a specific memory address. The physical location of the RAM device mapped in to that memory address depends on the type of system, the number and type of memory boards installed, and type of memory device used (256-kb or 1-mb RAMs).

The first 1 MB of RAM in the system is mapped into various areas of the system memory map. The common configuration is that the first 640 KB is the base memory. The next 256 KB is used by the COMPAQ Expanded Memory Management program and VDISK. The last 128 KB is reserved for system use.

The base memory size is configured on the memory board to 256 KB, 512 KB, or 640 KB. When the base memory size is reduced, the RAM normally assigned to the base memory is mapped into the COMPAQ Built-in Memory space. Table A-13 lists the memory-error code XX values for the various configurations.

Table A-13. XX Values

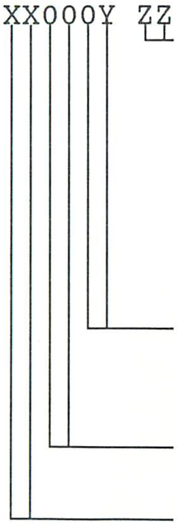
Base Memory Size	COMPAQ Built-in Memory Size	XX Values for COMPAQ Built-in Memory
256 KB	640 KB (256 KB + 384 KB)	F4 to FD
512 KB	384 KB (256 KB + 128 KB)	F8 to FD
640 KB	256 KB	FA to FD Factory Setting

Use Table A-14 to determine which of the memory-error tables to use to find the suspected defective chip.

Table A-14. DESKPRO 386 Memory Configurations

Error Code XX Value	Memory Device Location
00 to 1F (0 to 2 MB)	System Memory Board
20 to 3F (2 to 4 MB)	1- to 2-Megabyte 32-bit Memory Board
20 to 9F (2 to 8 MB)	4- to 8-Megabyte 32-bit Memory Board
F4 to FF (15 to 16 MB)	System Memory Board

Memory error codes are in the format XX000Y ZZ.



This value specifies which bits within a byte are bad
00 = parity bit
01 = data bit 0
02 = data bit 1
04 = data bit 2
08 = data bit 3
10 = data bit 4
20 = data bit 5
40 = data bit 6
80 = data bit 7

00 = byte 01 or bank 0
01 = byte 02 or bank 1
02 = byte 03 or bank 2
03 = byte 04 or bank 3

00 = always

This value specifies the 64-KB segment in which an error is detected. This value ranges from 00h to FFh, where FFh equals 16 MB. Memory banks using 256-kb RAMs contain sixteen 64-KB segments (1 MB).
Memory banks using 1-mb RAMs contain sixty-four 64-KB segments (4 MB).

The ZZ value is in a nibble format, which means that the left digit and the right digit are logically separate--each digit represents the state of four bits of the byte. When more than one bit is bad, each digit represents the sum of the values from the bad chips. Table A-15 shows some sample ZZ values:

Table A-15. Memory Error Code Definitions

ZZ(hex)	
11	Data bits 4 and 0
AE	Data bits 7, 5, 3, 2, and 1
FF	All data bits are bad

Appendix B

INTERNATIONAL KEYBOARDS

Appendix B
INTERNATIONAL KEYBOARDS

This appendix shows the international versions of the COMPAQ Enhanced Keyboard and the COMPAQ 84-Key Keyboard. Figures B-1 through B-10 show the versions by country in alphabetic order.

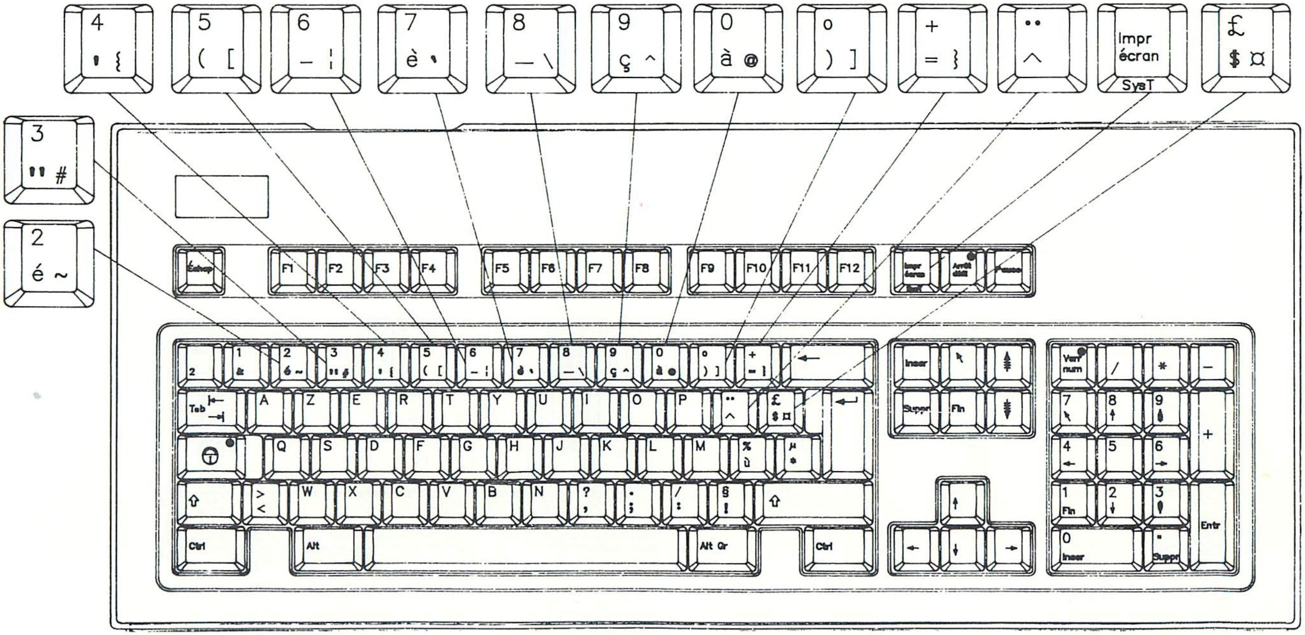


Figure B-1. French Enhanced Keyboard

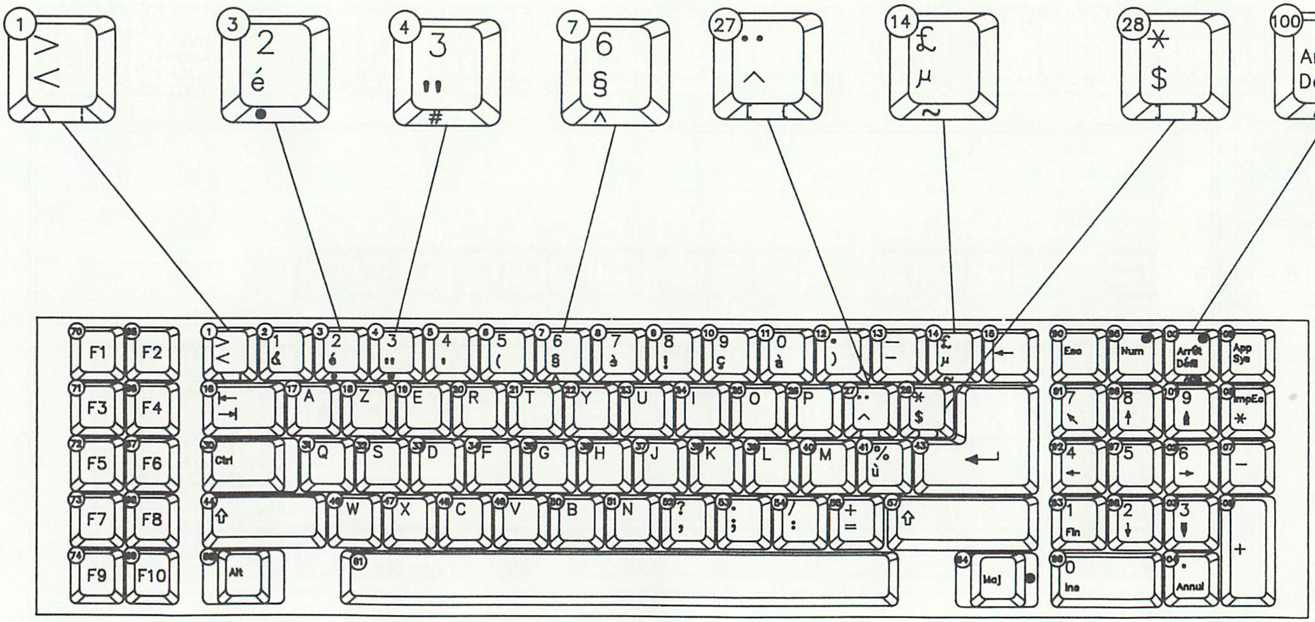


Figure B-2. French 84-Key Keyboard

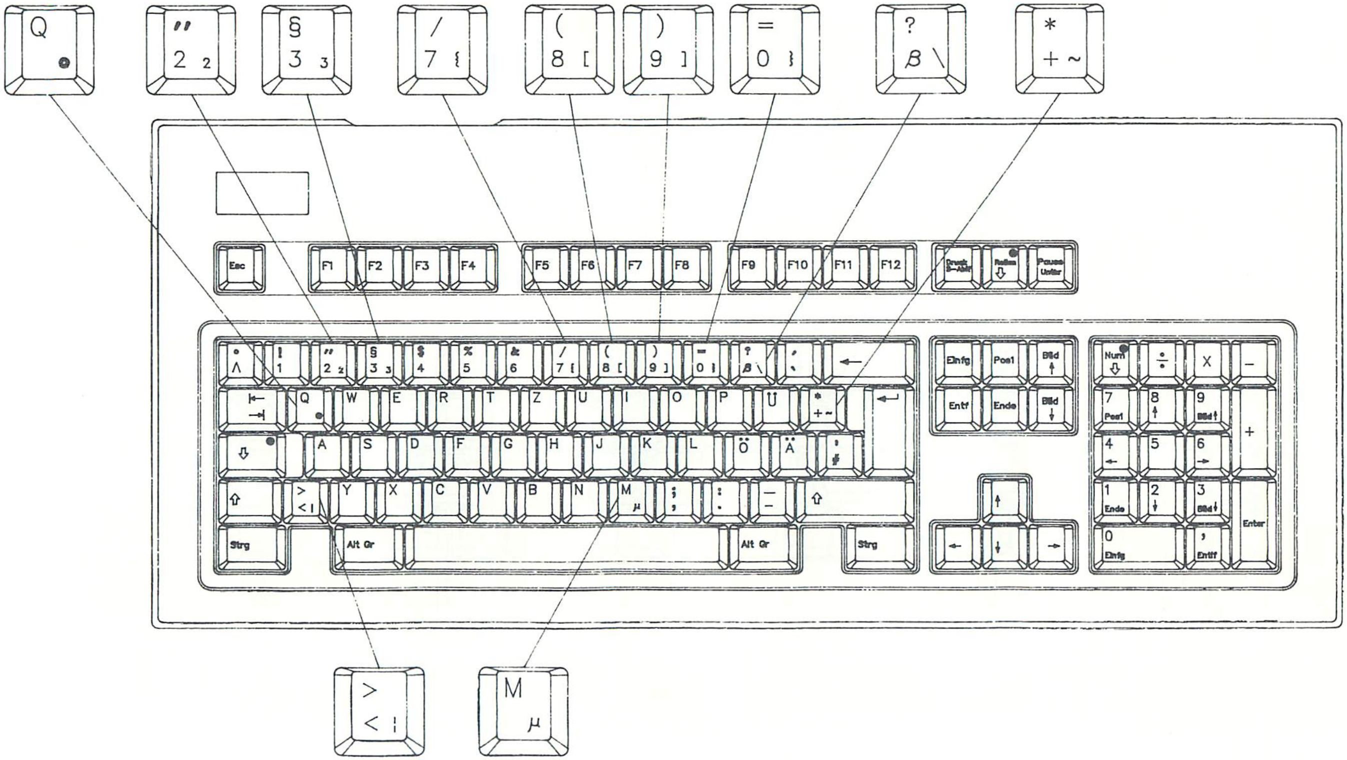


Figure B-3. German Enhanced Keyboard

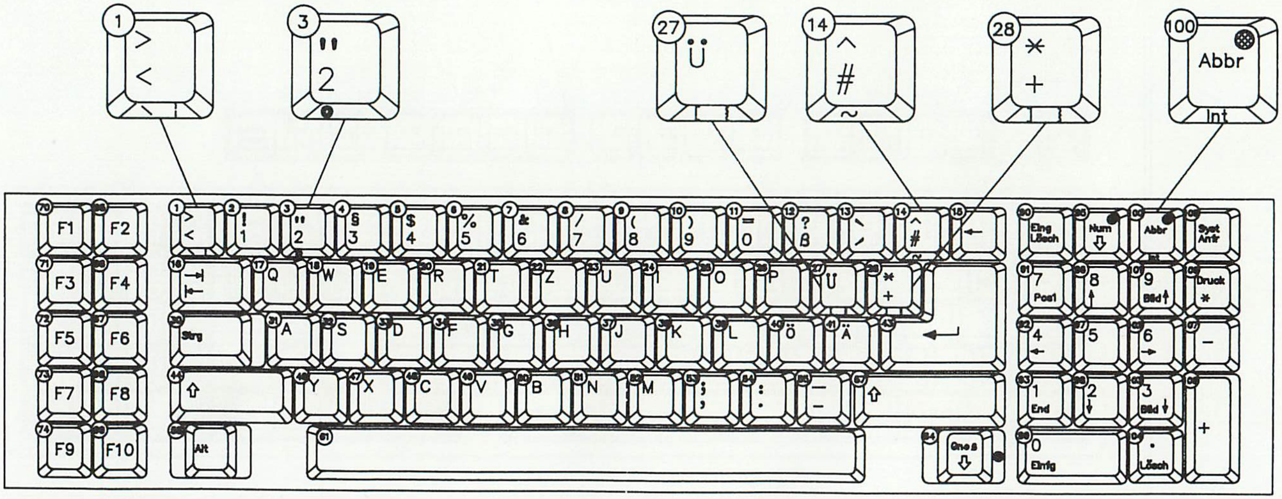


Figure B-4. German 84-Key Keyboard

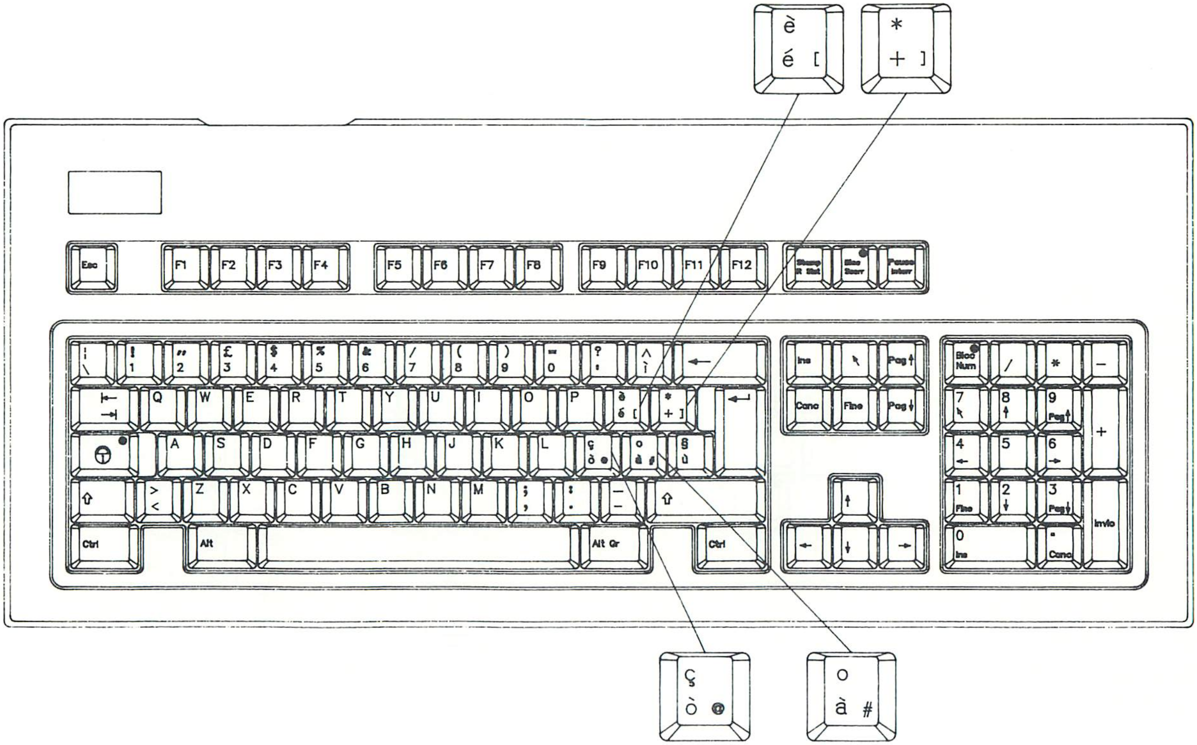


Figure B-5. Italian Enhanced Keyboard

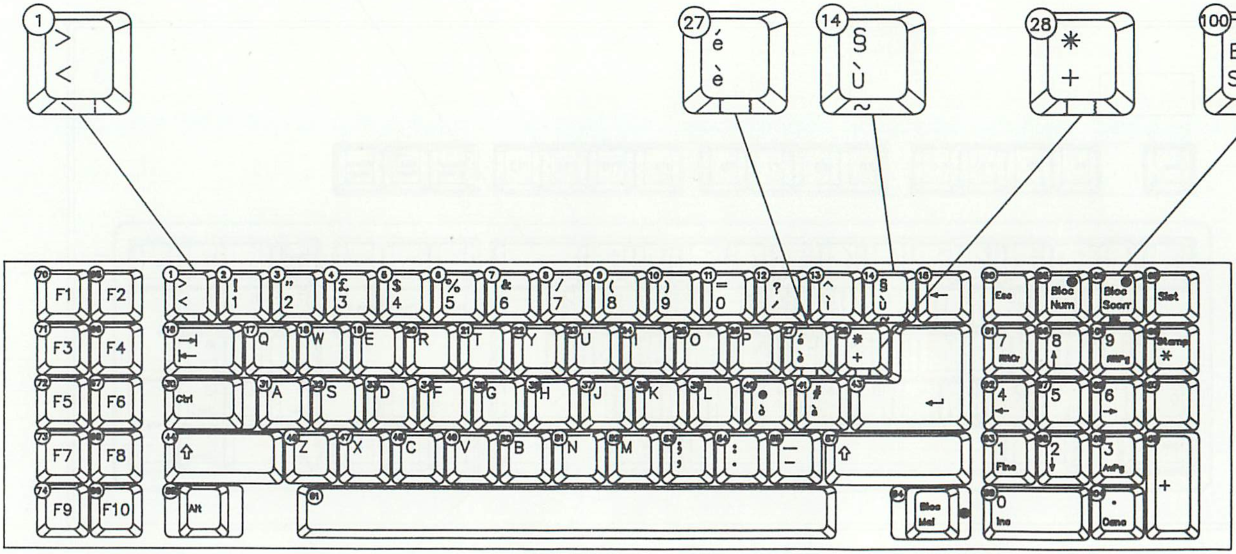


Figure B-6. Italian 84-Key Keyboard

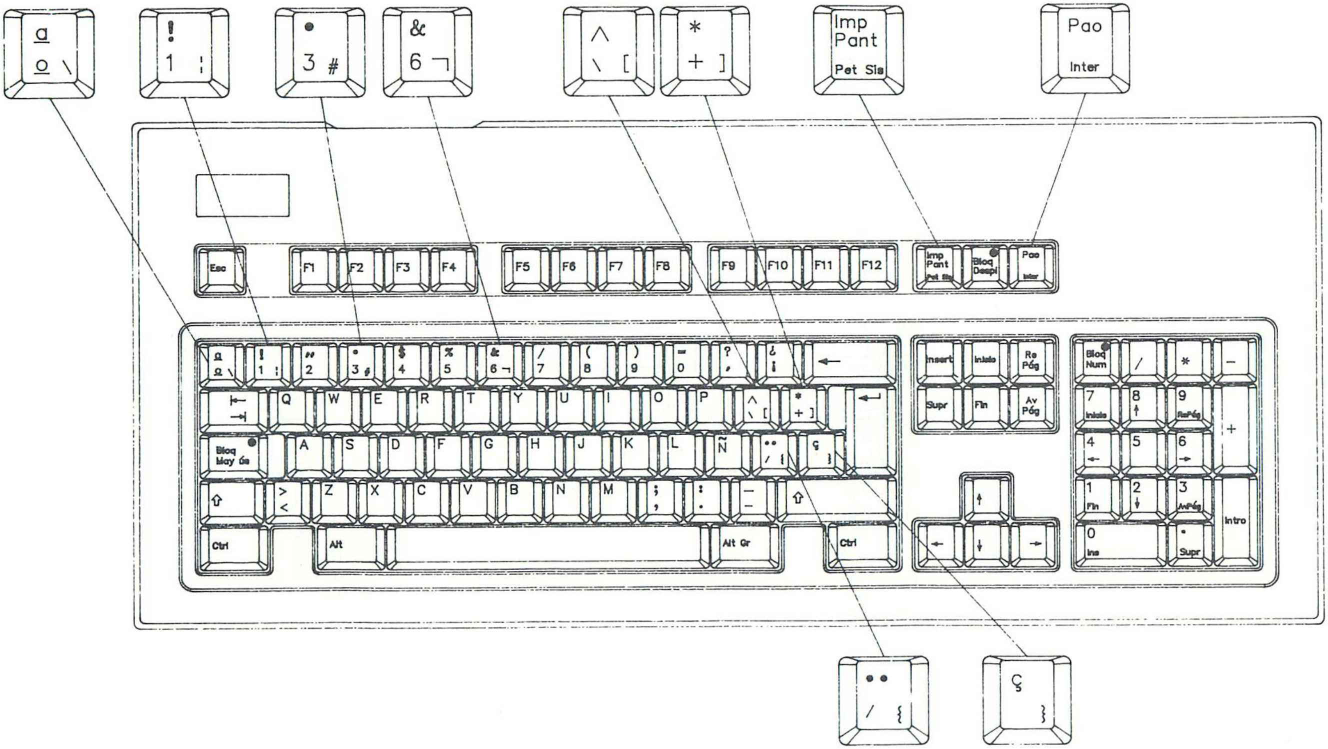


Figure B-7. Spanish Enhanced Keyboard

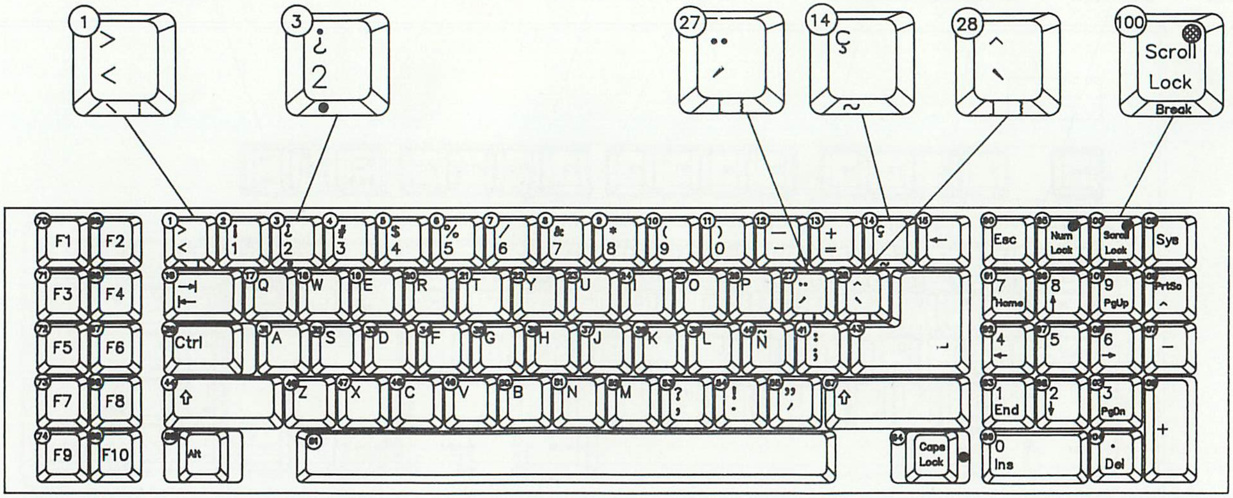


Figure B-8. Spanish 84-Key Keyboard

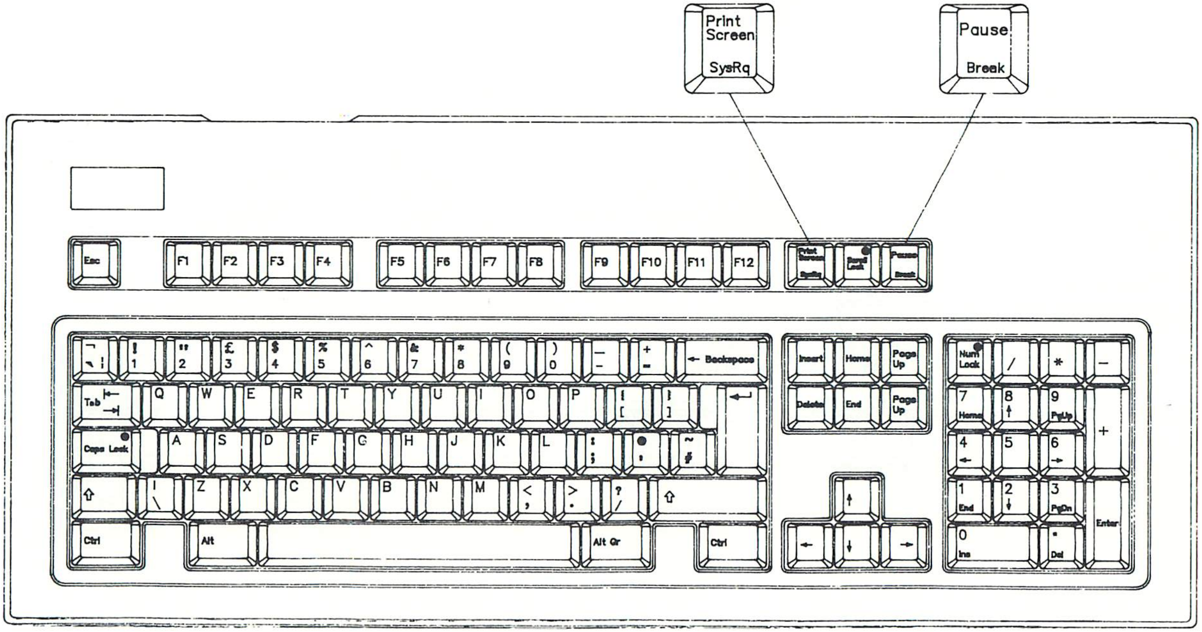


Figure B-9. United Kingdom Enhanced Keyboard

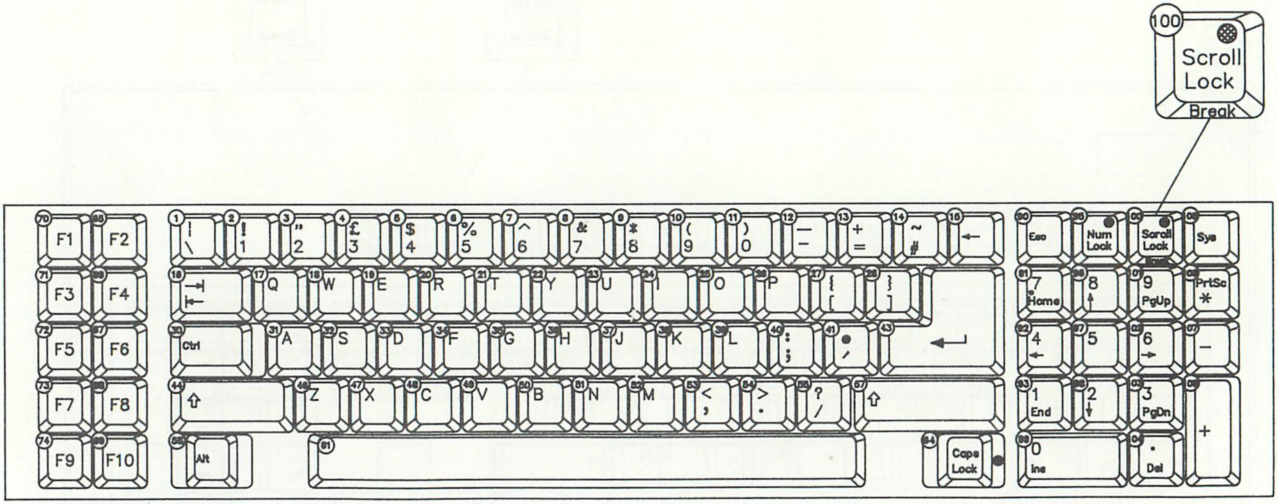


Figure B-10. United Kingdom 84-Key Keyboard

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